

APPLICATION  
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TITLE: LIGHT-EMITTING DEVICE

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# LIGHT-EMITTING DEVICE

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to an EL panel in which an EL element formed  
5 on a substrate is sealed between the substrate and a cover member. Further, the  
present invention relates to an EL module in which an IC is mounted in the EL  
panel. Incidentally, in the present specification, the EL panel and the EL module are  
generally referred to as a light-emitting device. The present invention further relates  
to an electronic instrument using the light-emitting device.

### 10 2. Description of the Related Art

In recent years, a technique for forming a TFT on a substrate has been greatly  
advanced, and application to an active matrix display device has been advanced.  
Especially, since a TFT using a polysilicon film has an electron field-effect mobility  
(also called mobility) higher than that of a TFT using a conventional amorphous  
15 silicon film, a high speed operation is possible. Thus, control of a pixel, which is  
conventionally performed by a driving circuit outside a substrate, can be performed  
by a driving circuit formed on the same substrate as the pixel.

In this sort of active matrix display device, various merits, such as reduction  
of manufacturing costs, miniaturization of an electro-optic device, improvement of  
20 a yield, and reduction of a throughput, can be obtained by forming various circuits  
and elements on the same substrate.

Further, research of an active matrix type light-emitting device including an

EL element as a self-luminous element has been actively carried out. The light-emitting device (EL display) including the EL element is also called an organic EL display (OELD: Organic EL Display) or an organic light-emitting diode (OLED: Organic Light-emitting Diode).

5       The light-emitting device is of a self-luminous type differently from a liquid crystal display device. The EL element has such a structure that a layer (hereinafter referred to as an EL layer) containing an organic compound is sandwiched between a pair of electrodes (anode and cathode), and the EL layer has normally a laminate structure. Typically, there is cited a laminate structure "hole transporting layer/light-emitting layer/electron transporting layer" proposed by Tang et al. of Eastman  
10       Kodak Company. This structure has a very high luminous efficiency, and most of the light-emitting devices on which research and development has been made at present adopt this structure.

      In the EL element, luminescence (Electro Luminescence) generated by  
15       application of an electric field is obtained, and it includes an anode layer, an EL layer, and a cathode layer. Luminescence in an organic compound includes light emission (fluorescence) generated when a single excited state returns to a ground state and light emission (phosphorescence) generated when a triplet excited state returns to the ground state, and the EL display of the present invention may use  
20       either light emission.

      In addition, there may be also adopted a structure in which laminating is made on an anode in the order of a hole injecting layer/a hole transporting layer/a light-emitting layer/an electron transporting layer or a hole injecting layer/a hole transporting layer/a light-emitting layer/an electron transporting layer/an electron  
25       injecting layer. The light-emitting layer may be doped with a fluorescent pigment

or the like.

In the present specification, all layers provided between a cathode and an anode are generally referred to as an EL layer. Thus, all of the foregoing hole injecting layer, hole transporting layer, light-emitting layer, electron transporting  
5 layer, electron injecting layer, and the like are included in the EL layer.

Besides, in the present specification, an element formed of an anode, an EL layer and a cathode is referred to as an EL element.

In a light-emitting device, a plurality of pixels are provided in a matrix form, and each of the plurality of pixels includes a thin film transistor (TFT) and an EL  
10 element. Fig. 4 is a circuit diagram of a pixel of a general light-emitting device. A pixel 400 includes a switching TFT 401, a current controlling TFT 402, an EL element 403, a source signal line 404, a gate signal line 405, a power supply line 406, and a capacitor 407.

A gate electrode of the switching TFT 401 is connected to the gate signal line  
15 405. One of a source region and a drain region of the switching TFT 401 is connected to the source signal line, and the other is connected to a gate electrode of the current controlling TFT 402. A source region of the current controlling TFT 402 is connected to the power supply line 406, and a drain region is connected to an anode or a cathode of the EL element 403.

20 In the case where the anode of the EL element 403 is connected to the drain region of the current controlling TFT 402, the anode of the EL element 403 becomes a pixel electrode, and the cathode becomes a counter electrode. On the contrary, in the case where the cathode of the EL element 403 is connected to the drain region of the current controlling TFT 402, the anode of the EL element 403  
25 becomes the counter electrode, and the cathode becomes the pixel electrode.

Note that, in the present specification, a potential difference between a potential of a pixel electrode and a potential of a counter electrode is called an EL driving voltage, and this EL driving voltage is applied to the EL layer.

Note that, as shown in Fig. 4, the capacitor 407 is provided to be connected  
5 to the current controlling TFT 402 and the power supply line 406.

The potential (power source potential) of the power supply line 406 is kept constant. The potential of the counter electrode of the EL element 403 is also kept constant. The potential of the counter electrode has a potential difference from the power source potential to such a degree that the EL element emits light when the  
10 power source potential is applied to the pixel electrode of the EL element.

The switching TFT 401 comes to have an on state by a selection signal inputted to the gate signal line 405. Incidentally, in the present specification, that a TFT comes to have an on state means that a drain current of the TFT comes to have a state of more than 0.

15 When the switching TFT 401 comes to have the on state, a video signal inputted from the source signal line 404 is inputted to the gate electrode of the current controlling TFT 402 through the switching TFT 401. Incidentally, in the present specification, the video signal means an analog signal including image information. Incidentally, that a signal is inputted to the gate electrode of the  
20 current controlling TFT 402 through the switching TFT 401 means that a carrier moves through an active layer of the switching TFT 401, and a potential of a video signal is given to the gate electrode of the current controlling TFT 402.

The amount of current flowing through the channel formation region of the current controlling TFT 402 is controlled by a gate voltage  $V_{gs}$  of a potential  
25 difference between the gate electrode and the source region of the current

controlling TFT 402. Thus, the potential given to the pixel electrode of the EL element 403 is determined by the height of the potential of the video signal inputted to the gate electrode of the current controlling TFT 402. The emission luminance of the EL element (luminance of light emitted from the EL element) is controlled  
5 by the height of the potential given to the pixel electrode. That is, the luminance of the EL element 403 is controlled by the potential of the video signal inputted to the source signal line 404 and a gradation display is carried out.

Fig. 5 shows the relation between the emission luminance ( $\text{cd/m}^2$ ) of an EL element and the current density ( $\text{mA/cm}^2$ ). The relation between the emission  
10 luminance of the EL element and the current density is linear. That is, when the current density of the EL element becomes high at a constant rate, the emission luminance of the EL element also becomes high at a constant rate. The current density is determined by a drain current  $I_d$  of the current controlling TFT 402.

Although it is desirable that TFTs formed in a pixel portion of a light-emitting  
15 device have the same characteristics, actually, the characteristics of the respective TFTs are subtly different from one another. Particularly, threshold  $V_{th}$  of a TFT is influenced by a difference in crystallinity of an active layer, an impurity unintentionally mixed in the active layer, and the like. Thus, there has been a case where  $V_{th}$  is different among the TFTs. Incidentally, in the present specification,  
20 the active layer means a semiconductor film including a source region, a drain region, and a channel forming region of a TFT.

When the value of the threshold  $V_{th}$  of the TFT becomes different, the value of the drain current  $I_d$  also becomes different. Expression 1 indicates the relation between the drain current  $I_d$  and the threshold  $V_{th}$ .

[Expression 1]

Where,  $\mu$  ( $\text{m}^2/\text{V}\cdot\text{sec}$ ) indicates a mobility of the TFT, and  $C_0$  ( $\text{F}/\text{cm}^2$ ) indicates a capacitance value per unit area of a capacitance (gate capacitance) formed by a gate electrode, an active layer and a gate insulating film of the TFT.

5 Besides,  $W$  and  $L$  indicate a channel width and a channel length of a channel forming region of the TFT, respectively, and its position is shown in Fig. 6. Fig. 6 is a view schematically showing the TFT, and the active layer includes a channel forming region 601, a source region 602, and a drain region 603. The channel forming region 601 is provided to be sandwiched between the source region 602 and  
10 the drain region 603. Although not shown in Fig. 6, there is also a case where an LDD region is provided between the channel forming region 601 and the source region 602 or the drain region 603.

A gate electrode 604 is provided over the channel forming region 601 through a gate insulating film (not shown). Note that in the present specification, the  
15 channel forming region 601 is included in a portion of an active layer 600 overlapping with the gate electrode 604 and indicates a portion where a channel is actually formed when a voltage is applied to the gate electrode 604.

The channel length  $L$  is a length of the channel forming region in the direction in which a carrier of a free electron or free hole flows. The channel width  $W$  is a  
20 length of the channel forming region in the direction vertical to the direction in which the carrier flows. Although the TFT shown in Fig. 6 has a single gate structure, in the case of a TFT having a multigate structure such as a double gate structure or a triple gate structure, the channel length  $L$  is defined as the sum of lengths of channel forming regions formed under all gate electrodes in the direction

in which the carrier flows.

As indicated by the expression 1, when the value of the threshold voltage  $V_{th}$  is varied, the value of the drain current  $I_d$  is also varied. Thus, if the value of the threshold voltage  $V_{th}$  of the current controlling TFT is different among pixels, even  
5 if video signals having the same potential are inputted to the respective pixels, the emission luminance of the EL element becomes different among the pixels. Note that in the present specification, to input a signal to a pixel means to input a signal to a gate electrode of a current controlling TFT through a switching TFT included in the pixel.

10 If the emission luminance is not uniform in all pixels of the light-emitting device, unevenness of luminance (uneven luminance) appears in an image displayed on the pixel portion and is visually recognized by an observer.

In order to suppress the foregoing uneven luminance, as shown in Fig. 18, a light-emitting device having a structure in which four TFTs are provided in a pixel  
15 is devised (SID'98 DIGEST 4.2 "Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display" R.M.A.Dawson etc.).

In Fig. 18, reference numeral 1701 designates a first thin film transistor; 1702, a second thin film transistor; 1703, a third thin film transistor; and 1704, a fourth thin film transistor. The emission luminance of an EL element 1705 is controlled by  
20 the first to fourth four thin film transistors.

When the first thin film transistor 1701 comes to have the on state by a selection signal inputted to a gate signal line (G), and the third thin film transistor 1703 comes to have the on state by a signal inputted to a first signal line (AZ), a gate electrode and a drain region of the second thin film transistor 1702 are short-  
25 circuited. Since the fourth thin film transistor 1704 is in an off state by a signal



inputted to a second signal line (AZB), a gate voltage  $V_{gs}$  of a voltage between the gate electrode and a source region of the second thin film transistor 1702 enters into a subthreshold region determined by a leak current.

Next, the third thin film transistor 1703 comes to have the off state by a signal  
5 inputted to the first signal line (AZ). Then, a video signal is inputted to a source signal line (S) and a potential of the video signal is given to the gate electrode of the second thin film transistor 1702 through the first thin film transistor 1701 having the on state. Accordingly, the gate voltage  $V_{gs}$  of the third thin film transistor 1703 becomes a potential obtained by adding the potential of the video signal to the gate  
10 voltage  $V_{gs}$  having entered into the subthreshold region.

Next, the first thin film transistor 1701 comes to have the off state by a selection signal inputted to the gate signal line (G). Then, the fourth thin film transistor 1704 comes to have the on state by a signal inputted to the second signal line (AZB). Since a current flowing through the channel forming region of the TFT  
15 depends on the value of the gate voltage  $V_{gs}$  of the third thin film transistor 1703, the current having the intensity corresponding to the potential of the video signal is inputted to a pixel electrode of the EL element 1705.

In the case of the light-emitting device having the above structure, in the case where video signals having the same potential are inputted to the source signal line,  
20 it is possible to prevent the potential given to the pixel electrode from being varied by the value of the threshold  $V_{th}$  of the second thin film transistor 1702. Thus, the uneven luminance of an image can be suppressed. However, if the number of thin film transistors provided in each pixel is increased, the opening ratio is lowered, and it becomes necessary to increase a current flowing through an EL element in order  
25 to obtain constant luminance. If the current flowing through the EL element is

increased, deterioration of the EL layer is accelerated, which is not preferable.

Besides, if the number of TFTs provided in a pixel is increased, there is a fear that yield of the light-emitting device itself is lowered.

### SUMMARY OF THE INVENTION

5        In view of the above, the present invention has an object to provide a light-emitting device in which the number of thin film transistors provided in each of pixels is restricted to two, and uneven luminance due to fluctuation in threshold voltage of current controlling TFTs included in the respective pixels can be suppressed.

10        The present inventors have considered that it is necessary to restrict a difference in emission luminance of respective pixels provided in a pixel portion to a certain constant range (for example, within  $\pm 5\%$ ) in order to prevent uneven luminance of an image from being visually recognized by an observer. Further, since uneven luminance is more noticeable between adjacent pixels, the present inventor  
15 et al. have considered that it is necessary that the difference in emission luminance between adjacent pixels is restricted to a range (for example, within  $\pm 3\%$ ) narrower than the difference of emission luminance between pixels which are not adjacent to each other.

For example, in order to restrict the difference in the emission luminance of  
20 the respective pixels to a range of  $\pm n\%$ , the following expression can be derived from the expression 1. When the expression 1 is modified, expression 2 is obtained.

[Expression 2]

A mobility  $\mu$  and a capacitance value  $C_0$  of a gate capacitance are values fixed at the point of time when a TFT is formed. When an EL element is made to emit light at desired emission luminance, since the relation between the emission  
5 luminance of the EL element and current density is linear, the value of a drain current  $I_d$  is also fixed. Thus, expression 3 is derived by replacing the right side of the expression 2 by a constant A.

[Expression 3]

In consideration of confining the difference in the emission luminance of the  
10 respective pixels to the range of  $\pm n\%$ , expression 4 and expression 5 are obtained from the expression 3. Threshold voltage  $V_{th}$  is an average of threshold voltages of current controlling TFTs of all pixels. The symbol  $\Delta V_{th}$  stands for a difference between an actual threshold voltage of each pixel and the threshold voltage  $V_{th}$ .

[Expression 4]

15 [Expression 5]

If  $V_{gs} - V_{th} = V'$ , expression 6 is derived from the expression 4 and the expression 5.

[Expression 6]

Here, expression 7 is obtained from the expression 3.

[Expression 7]

Thus, expression 8 is derived from the expression 6 and the expression 7.

[Expression 8]

5        When the expression 8 is solved with respect to  $W/L$ , expression 9 is obtained.

[Expression 9]

10        If the gate voltage  $V_{gs}$  is too high, the TFT itself is deteriorated, so that it is necessary that the gate voltage  $V_{gs}$  has such an intensity that an element is not broken. When a value of the gate voltage  $V_{gs}$  immediately before the element is broken is made  $V_{gs(max)}$ , the following expression 10 is derived from the expression 3. Note that it is necessary that  $V_{gs(max)}$  is about 25 V, and is desirably 10 V or less.

[Expression 10]

15        Expression 11 is obtained from the above expressions 9 and 10.

[Expression 11]

If the values of  $\Delta V_{th}$  and  $W/L$  are determined in the range where the above expression 8 or 11 is satisfied, the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm n\%$ .

For example, in the case where the value of the ratio  $W/L$  of the channel  
5 width  $W$  to the channel length  $L$  is fixed by a problem of design, the range of the fluctuation  $\Delta V_{th}$  of the threshold voltage is determined by the expression 8 from the value of the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$ .

In the case where the fluctuation  $\Delta V_{th}$  of the threshold voltage is fixed by a fabricating process of TFTs, the range of the ratio  $W/L$  of the channel width  $W$  to  
10 the channel length  $L$  is determined by the expression 11 from the value of the fluctuation  $\Delta V_{th}$  of the threshold voltage.

By the above structure, in the light-emitting device of the present invention, the number of thin film transistors provided in each of pixels is made two to prevent a drop in an opening ratio, and it becomes possible to suppress uneven luminance  
15 due to fluctuation in the threshold voltage of the current controlling TFT included in each of the pixels.

Note that the above expressions 4 to 11 are obtained under the assumption that the difference in the emission luminance of the respective pixels is restricted to the range of  $\pm n\%$ . In the case where the difference in the emission luminance  
20 between adjacent pixels is restricted to the range of  $\pm 5\%$ , the relation between the fluctuation  $\Delta V_{th}$  of the threshold voltage and the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$  is expressed by the following expressions 12 and 13.

[Expression 12]

[Expression 13]

If the values of  $\Delta V_{th}$  and  $W/L$  are determined within the range where the above expression 12 or 13 is satisfied, the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm 5\%$ .

5        For example, in the case where the fluctuation  $\Delta V_{th}$  of the threshold voltage is fixed by a fabricating process of TFTs, the range of the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$  is determined by the expression 12 from the value of the fluctuation  $\Delta V_{th}$  of the threshold voltage.

      Besides, in the case where the value of the ratio  $W/L$  of the channel width  $W$   
10 to the channel length  $L$  is fixed by a problem of design, the range of the fluctuation  $\Delta V_{th}$  of the threshold voltage is determined by the expression 13 from the value of the ratio  $W/L$  of the channel width  $W$  and the channel length  $L$ .

      By the above structure, in the light-emitting device of the present invention, the number of thin film transistors provided in each of the pixels is made two to  
15 prevent a drop in the opening ratio, and it becomes possible to suppress uneven luminance due to fluctuation in threshold voltage of current controlling TFTs included in the respective pixels.

      In the case where the difference in the emission luminance of the respective pixels is restricted to the range of  $\pm 3\%$ , the relation between the fluctuation  $\Delta V_{th}$   
20 of the threshold voltage and the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$  is expressed by the following expressions 14 and 15.

[Expression 14]

[Expression 15]

If the values of  $\Delta V_{th}$  and  $W/L$  are determined within the range where the above expression 14 or 15 is satisfied, the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm 3\%$ .

5        For example, in the case where the fluctuation  $\Delta V_{th}$  of the threshold voltage is fixed by a fabricating process of TFTs, the range of the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$  is determined by the expression 14 from the value of the fluctuation  $\Delta V_{th}$  of the threshold voltage.

Besides, in the case where the value of the ratio  $W/L$  of the channel width  $W$   
10 to the channel length  $L$  is fixed by a problem of design, the range of the fluctuation  $\Delta V_{th}$  of the threshold voltage is determined by the expression 15 from the value of the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$ .

By the above structure, in the light-emitting device of the present invention, the number of thin film transistors provided in each of pixels is made two to  
15 suppress a drop in the opening ratio, and it becomes possible to suppress uneven luminance due to fluctuation in threshold voltage of current controlling TFTs included in the respective pixels.

The structure of the present invention is as follows:

According to the present invention, there is provided a light-emitting device  
20 including a plurality of pixels, wherein:

the plurality of pixels include a plurality of switching TFTs, a plurality of current controlling TFTs, and a plurality of EL elements,

emission luminance of the EL elements are controlled by video signals inputted to gate electrodes of the plurality of current controlling TFTs through the plurality

of switching TFTs,

the plurality of current controlling TFTs respectively include active layers, gate insulating films on the active layers, and gate electrodes on the gate insulating films,

5 the active layers respectively include source regions, drain regions, and channel forming regions provided between the source regions and the drain regions, and

when a drain current of the plurality of current controlling TFTs when the luminance of the EL element becomes maximum is  $I_d$ , a mobility is  $\mu$ , a gate capacitance per unit area is  $C_o$ , a maximum gate voltage is  $V_{gs(max)}$ , a channel width  
10 is  $W$ , a channel length is  $L$ , an average value of a threshold voltage is  $V_{th}$ , a deviation from the average value of the threshold voltage is  $\Delta V_{th}$ , and a difference in the emission luminance of the plurality of EL elements is within a range of  $\pm n\%$ , Expression 16 is satisfied.

[Expression 16]

15 According to the present invention, there is provided a light-emitting device including a plurality of pixels, wherein:

the plurality of pixels include a plurality of switching TFTs, a plurality of current controlling TFTs, and a plurality of EL elements,

emission luminance of the EL elements are controlled by video signals inputted  
20 to gate electrodes of the plurality of current controlling TFTs through the plurality of switching TFTs,

the plurality of current controlling TFTs respectively include active layers, gate insulating films on the active layers, and gate electrodes on the gate insulating



films,

the active layers respectively include source regions, drain regions, and channel forming regions provided between the source regions and the drain regions, and

when a drain current of the plurality of current controlling TFTs when the  
5 luminance of the EL element becomes maximum is  $I_d$ , a mobility is  $\mu$ , a gate capacitance per unit area is  $C_o$ , a maximum gate voltage is  $V_{gs(max)}$ , a channel width is  $W$ , a channel length is  $L$ , an average value of a threshold voltage is  $V_{th}$ , a deviation from the average value of the threshold voltage is  $\Delta V_{th}$ , and a difference in the emission luminance of the plurality of EL elements is within a range of  $\pm n\%$ ,  
10 Expression 17 is satisfied.

[Expression 17]

According to the present invention, a light-emitting device includes a source signal line driving circuit, a gate signal line driving circuit, a pixel portion, a plurality of source signal lines, a plurality of gate signal lines, and power supply lines,  
15 wherein:

the pixel portion includes a plurality of pixels,

the plurality of pixels respectively include a plurality of switching TFTs, a plurality of current controlling TFTs, and a plurality of EL elements,

the EL elements respectively include anodes, cathodes, and EL layers provided  
20 between the cathodes and the anodes,

gate electrodes of the plurality of switching TFTs are connected to the plurality of gate lines,

ones of source regions and drain regions of the plurality of switching TFTs are

connected to the plurality of source signal lines, and the other ones are connected to gate electrodes of the plurality of current controlling TFTs,

source regions of the plurality of current controlling TFTs are connected to the power supply lines, and drain regions are connected to the anodes or the cathodes  
5 of the EL elements,

video signals are inputted to the plurality of source signal lines by the source signal line driving circuit,

the video signals inputted to the plurality of source signal lines are inputted to the gate electrodes of the plurality of current controlling TFTs through the plurality  
10 of switching TFTs so that emission luminance of the plurality of EL elements is controlled,

the plurality of current controlling TFTs respectively include active layers, gate insulating films on the active layers, and gate electrodes on the gate insulating films,

15 the active layers respectively include source regions, drain regions, and channel forming regions provided between the source regions and the drain regions, and

when a drain current of the plurality of current controlling TFTs when the luminance of the EL element becomes maximum is  $I_d$ , a mobility is  $\mu$ , a gate capacitance per unit area is  $C_o$ , a maximum gate voltage is  $V_{gs(max)}$ , a channel width  
20 is  $W$ , a channel length is  $L$ , an average value of a threshold voltage is  $V_{th}$ , a deviation from the average value of the threshold voltage is  $\Delta V_{th}$ , and a difference in the emission luminance of the plurality of EL elements is within a range of  $\pm n\%$ , Expression 18 is satisfied.

[Expression 18]

According to the present invention, a light-emitting device includes a source signal line driving circuit, a gate signal line driving circuit, a pixel portion, a plurality of source signal lines, a plurality of gate signal lines, and power supply lines, wherein

- 5       the pixel portion includes a plurality of pixels,  
          the plurality of pixels respectively includes a plurality of switching TFTs, a plurality of current controlling TFTs, and a plurality of EL elements,  
          the EL elements respectively include anodes, cathodes, and EL layers provided between the cathodes and the anodes,
- 10       gate electrodes of the plurality of switching TFTs are connected to the plurality of gate lines,  
          ones of source regions and drain regions of the plurality of switching TFTs are connected to the plurality of source signal lines, and the other ones are connected to gate electrodes of the plurality of current controlling TFTs,
- 15       source regions of the plurality of current controlling TFTs are connected to the power supply lines, and drain regions are connected to the anodes or the cathodes of the EL elements,  
          video signals are inputted to the plurality of source signal lines by the source signal line driving circuit,
- 20       the video signals inputted to the plurality of source signal lines are inputted to the gate electrodes of the plurality of current controlling TFTs through the plurality of switching TFTs so that emission luminance of the plurality of EL elements is controlled,  
          the plurality of current controlling TFTs respectively include active layers, gate
- 25       insulating films on the active layers, and gate electrodes on the gate insulating

films,

the active layers respectively include source regions, drain regions, and channel forming regions provided between the source regions and the drain regions, and

when a drain current of the plurality of current controlling TFTs when the  
5 luminance of the EL element becomes maximum is  $I_d$ , a mobility is  $\mu$ , a gate capacitance per unit area is  $C_o$ , a maximum gate voltage is  $V_{gs(max)}$ , a channel width is  $W$ , a channel length is  $L$ , an average value of a threshold voltage is  $V_{th}$ , a deviation from the average value of the threshold voltage is  $\Delta V_{th}$ , and a difference in the emission luminance of the plurality of EL elements is within a range of  $\pm n\%$ ,  
10 Expression 19 is satisfied.

[Expression 19]

The light-emitting device may be characterized in that the current controlling TFTs are n-channel TFTs and the drain regions of the current controlling TFTs are connected to the cathodes of the EL elements.

15 The light-emitting device may be characterized in that the current controlling TFTs are p-channel TFTs and the drain regions of the current controlling TFTs are connected to the anodes of the EL elements.

According to the present invention, there is provided a light-emitting device including a plurality of pixels, wherein:

20 the plurality of pixels include a plurality of switching TFTs, a plurality of current controlling TFTs, and a plurality of EL elements,

emission luminance of the EL elements is controlled by video signals inputted to gate electrodes of the plurality of current controlling TFTs through the plurality

of switching TFTs,

the plurality of current controlling TFTs respectively include active layers, gate insulating films on the active layers, and gate electrodes on the gate insulating films,

5 the active layers respectively include source regions, drain regions, and channel forming regions provided between the source regions and the drain regions,

when a drain current of the plurality of current controlling TFTs when the luminance of the EL element becomes maximum is  $I_d$ , a mobility is  $\mu$ , a gate capacitance per unit area is  $C_o$ , a maximum gate voltage is  $V_{gs(max)}$ , a channel width  
10 is  $W$ , a channel length is  $L$ , an average value of a threshold voltage is  $V_{th}$ , a deviation from the average value of the threshold voltage is  $\Delta V_{th}$ , and a difference in the emission luminance of the plurality of EL elements is within a range of  $\pm n\%$ ,  
Expression 20 is satisfied, and

a ratio of the channel width  $W$  to the channel length  $L$  in each of the pixels  
15 is different from one another according to a color displayed by each of the pixels.

[Expression 20]

According to the present invention, there is provided a light-emitting device including a plurality of pixels, wherein:

the plurality of pixels include a plurality of switching TFTs, a plurality of  
20 current controlling TFTs, and a plurality of EL elements,

emission luminance of the EL elements is controlled by video signals inputted to gate electrodes of the plurality of current controlling TFTs through the plurality of switching TFTs,

the plurality of current controlling TFTs respectively include active layers, gate insulating films on the active layers, and gate electrodes on the gate insulating films,

the active layers respectively include source regions, drain regions, and channel forming regions provided between the source regions and the drain regions,

when a drain current of the plurality of current controlling TFTs when the luminance of the EL element becomes maximum is  $I_d$ , a mobility is  $\mu$ , a gate capacitance per unit area is  $C_o$ , a maximum gate voltage is  $V_{gs(max)}$ , a channel width is  $W$ , a channel length is  $L$ , an average value of a threshold voltage is  $V_{th}$ , a deviation from the average value of the threshold voltage is  $\Delta V_{th}$ , and a difference in the emission luminance of the plurality of EL elements is within a range of  $\pm n\%$ , Expression 21 is satisfied, and

a ratio of the channel width  $W$  to the channel length  $L$  in each of the pixels is different from one another according to a color displayed by each of the pixels.

[Expression 21]

The light-emitting device may be characterized in that the difference in the emission luminance of the plurality of EL elements is within a range of  $\pm 5\%$ .

The light-emitting device may be characterized in that the difference in the emission luminance of the plurality of EL elements is within a range of  $\pm 3\%$ .

The light-emitting device may be characterized in that the maximum gate voltage is 25 V.

The light-emitting device may be characterized in that the maximum gate voltage is 25 V and a ratio of the channel width  $W$  to the channel length  $L$  of each

of the plurality of current controlling TFTs is  $2.26 \times 10^{-3} \leq W/L \leq 0.214$ .

The gate capacitance is formed in a portion where the channel forming region, the gate insulating film, and the gate electrode overlap with one another in each of the current controlling TFTs.

5        A video camera characterized by using the light-emitting device.

      An image reproduction apparatus characterized by using the light-emitting device.

      A head mount display characterized by using the light-emitting device.

      A personal computer characterized by using the light-emitting device.

10                    BRIEF DESCRIPTION OF THE DRAWINGS

      Fig. 1 is a circuit diagram of a pixel portion of a light-emitting device of Embodiment 1;

      Fig. 2 is an upper plane block diagram of the light-emitting device of Embodiment 1;

15        Fig. 3 is a timing chart showing a driving method of the light-emitting device of Embodiment 1;

      Fig. 4 is a circuit diagram of a light-emitting device of the present invention;

      Fig. 5 is a correlation view of emission luminance of an EL element and current  
20    density;

      Fig. 6 is a top view of a TFT;

      Figs. 7A to 7D are views showing fabricating steps of a light-emitting device of Embodiment 3;

Figs. 8A to 8D are views showing fabricating steps of the light-emitting device of Embodiment 3;

Figs. 9A to 9C are views showing fabricating steps of the light-emitting device of Embodiment 3;

5 Figs. 10A and 10B are views showing fabricating steps of the light-emitting device of Embodiment 3;

Figs. 11A and 11B are a top view and a sectional view of a light-emitting device of Embodiment 4;

Figs. 12A to 12C are circuit diagrams of pixels of light-emitting devices of  
10 Embodiment 5;

Fig. 13 is a circuit diagram of a source signal line driving circuit of Embodiment 6;

Figs. 14A and 14B are equivalent circuit diagrams of a level shift and an analog switch of Embodiment 6;

15 Fig. 15 is a top view of a pixel of Embodiment 7;

Figs. 16A to 16F are views of electronic apparatuses each using a light-emitting device of Embodiment 13;

Figs. 17A and 17B are views of electronic apparatuses each using a light-emitting device of Embodiment 13;

20 Fig. 18 is a circuit diagram of a pixel portion of a convention light-emitting device;

Fig. 19 is a view of a spin coater used when a light-emitting device of Embodiment 8 is fabricated; and

Fig. 20 is a sectional detailed view of a light-emitting device of Embodiment  
25 10.



## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described below.

### [Embodiment 1]

In this embodiment, an example in which the present invention is applied to  
5 an actual light-emitting device by using the above described expressions 8 and 11  
will be described.

In this embodiment, a light-emitting device having a resolution of QVGA of  
320 × 240 and a size of 4 inches will be exemplified.

A pixel size of the 4-inch QVGA light-emitting device is about 84 μm × 252  
10 μm. When an attempt to obtain definite luminance is made, the intensity of current  
flowing through an EL element per unit area is determined. In this embodiment, it  
is made 3 mA/cm<sup>2</sup> per unit area.

Thus, a drain current  $I_d$  of a current controlling TFT included in each of  
pixels is expressed by the following expression 22.

### 15 [Expression 22]

The above expression indicates a value of the drain current  $I_d$  of the current  
controlling TFT when the opening ratio of the light-emitting device is 100 %.  
Actually, in almost all cases, the opening ratio of the light-emitting device is not 100  
%. As the opening ratio of the light-emitting device is lowered, the value of an  
20 actually required drain current  $I_d$  becomes large. For example, when the opening  
ratio of the light-emitting device of this embodiment is 30 %, the value of the

actually required drain current  $I_d$  is obtained by the following expression 23.

[Expression 23]

When the mobility of the current controlling TFT of the light-emitting device used in this embodiment is  $\mu = 100 \text{ (m}^2/\text{V}\cdot\text{sec)}$ , and the capacitance value of gate  
5 capacitance is  $C_o = 3 \times 10^{-8} \text{ (F/cm}^2\text{)}$ , a constant A is obtained from expression 24.

[Expression 24]

A difference in emission luminance of the respective pixels is made to be restricted to a range of, for example,  $\pm 5\%$ . When the gate voltage  $V_{gs(\max)}$   
10 immediately before the TFT is broken is made 25 V, and the value of the threshold voltage  $V_{th}$  is made 0 V, the following expressions 25 and 26 are obtained from the expressions 8 and 11.

[Expression 25]

[Expression 26]

15 In the light-emitting device of the present invention, the values of  $\Delta V_{th}$  and  $W/L$  are determined in the range where the above expression 25 or 26 is satisfied, and the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm 5\%$ .

For example, in the case where the value of the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$  is fixed to 7.5 by a problem of design, when  $W/L = 1/7.5$  is substituted in the expression 25, the following expression 27 is obtained.

5 [Expression 27]

If the fluctuation  $\Delta V_{th}$  of the threshold voltage is determined so that the expression 27 is satisfied, the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm 5\%$ .

Besides, for example, it is assumed that the fluctuation  $\Delta V_{th}$  of the threshold  
10 voltage is fixed by a fabricating process of TFTs, and  $\Delta V_{th} = 0.1$  V. When  $\Delta V_{th} = 0.1$  V is substituted in the expression 26, the following expression 28 is obtained.

[Expression 28]

If the ratio  $W/L$  of the channel length  $L$  and the channel width  $W$  is  
15 determined so that the expression 28 is satisfied, the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm 5\%$ .

By the above structure, in the light-emitting device of the present invention, the number of thin film transistors provided in each of the pixels is made two to prevent a drop in the opening ratio, and it becomes possible to suppress uneven  
20 luminance due to fluctuation in the threshold voltage of the current controlling TFTs included in the respective pixels.

Note that in this embodiment, although the description has been given of the example in which the fluctuation of the drain current  $I_d$  is suppressed to the range of  $\pm 5\%$ , the present invention is not limited to this numerical value.

[Embodiment 2]

5        A driving method of a light-emitting device of the present invention will be described with reference to Figs. 1 to 3.

Fig. 1 is a top view of a light-emitting device of the present invention. Reference numeral 101 designates a source signal line driving circuit; 102, a gate signal line driving circuit; and 103, a pixel portion. In this embodiment, although  
10    one source signal line driving circuit and one gate signal line driving circuit are provided, the present invention is not limited to this structure. Two source signal line driving circuits may be provided, or two gate signal line driving circuits may be provided.

The source signal line driving circuit 101 includes a shift register 101\_1, a level  
15    shift 101\_2, and a sampling circuit 101\_3. Note that the level shift 101\_2 has only to be used as the need arises, and it may not be always used. Besides, although this embodiment is made to have such a structure that the level shift 101\_2 is provided between the shift register 101\_1 and the sampling circuit 101\_3, the present invention is not limited to this structure. A structure may be such that the level  
20    shift 101\_2 is incorporated in the shift register 101\_1.

In the pixel portion 103, a source signal line 104 connected to the source signal line driving circuit 101 intersects with a gate signal line 106 connected to the gate signal line driving circuit 102. A power supply line 105 is connected to a power source so that it is kept a constant potential (power source potential).

The gate signal line driving circuit 102 includes a shift register and a buffer (both are not shown). It may include a level shift.

A clock signal (CLK) as a panel control signal, and a start pulse (SP) are inputted to the shift register 101\_1. A sampling signal for sampling a video signal  
5 is outputted from the shift register 101\_1. The outputted sampling signal is inputted to the level shift 101\_2, and is outputted after the amplitude of its potential becomes high.

The sampling signal outputted from the level shift 101\_2 is inputted to the sampling circuit 101\_3. At the same time, the video signal is inputted to the  
10 sampling circuit 101\_3 through a video signal line (not shown).

In the sampling circuit 101\_3, the inputted video signal is sampled by the sampling signal, and is inputted to the source signal line 104.

Fig. 2 shows a structure of the pixel portion 103 of the light-emitting device shown in Fig. 1. A gate signal line (106\_1 to 106\_y) through which a selection  
15 signal from the gate signal line driving circuit 102 is inputted is connected to a gate electrode of a switching TFT 107 included in each of pixels. Besides, one of a source region and a drain region of the switching TFT 107 included in each of the pixels is connected to a source signal line (104\_1 to 104\_x) through which the video signal is inputted, and the other is connected to a gate electrode of a current  
20 controlling TFT 108 included in each of the pixels and a capacitor 110 included in each of the pixels, respectively.

A source region of the current controlling TFT 108 included in each of the pixels is connected to a power supply line (105\_1 to 105\_x) and a drain region is connected to an anode or a cathode of an EL element 109. The power supply line  
25 (105\_1 to 105\_x) is connected to the capacitor 110 included in each of the pixels.

Note that in this embodiment, although the structure including the capacitor 110 is shown, the capacitor 110 may not be necessarily provided.

The EL element 109 includes an anode, a cathode, and an EL layer provided between the anode and the cathode. In the case where the anode of the EL element 5 109 is connected to the drain region of the current controlling TFT 108, the anode of the EL element 109 becomes a pixel electrode, and the cathode becomes a counter electrode. On the contrary, in the case where the cathode of the EL element 109 is connected to the drain region of the current controlling TFT 108, the anode of the EL element 109 becomes a counter electrode, and the cathode 10 becomes a pixel electrode.

Fig. 3 shows a timing chart in the case where the light-emitting device shown in Figs. 1 and 2 is driven by an analog system. A period from a point when one gate signal line is selected to a point when another gate signal line is next selected is called one line period (L). Note that in the present specification, that a gate signal 15 line is selected means that a selection signal having such a potential that a switching TFT comes to have an on state is inputted to the gate signal line.

A period from a point when one image is displayed to a point when a next image is displayed corresponds to one frame period (F). In the case of the light-emitting device shown in Fig. 2, since there are y gate signal lines 104, y line periods 20 (L1 to Ly) are provided in one frame period.

First, the potential (power source potential) of the power supply line (105\_1 to 105\_x) is kept constant. The potential of the counter electrode is also kept constant. The potential of the counter electrode has a potential difference from the power source potential to such a degree that the EL element emits light when the 25 power source potential is applied to the pixel electrode of the EL element.

In a first line period (L1), the gate signal line 106\_1 is selected by the selection signal inputted from the gate signal line driving circuit 102 through the gate signal line 106\_1, and all the switching TFTs 107 connected to the gate signal line 106\_1 come to have on states. Then, video signals are sequentially inputted to the source  
5 signal lines (104\_1 to 104\_x) from the source signal line driving circuit 101. The video signals inputted to the source signal lines (104\_1 to 104\_x) are respectively inputted to the gate electrodes of the current controlling TFTs 108 through the switching TFTs 107.

The amount of current flowing through a channel forming region of the  
10 current controlling TFT 108 is controlled by a gate voltage  $V_{gs}$  of a potential difference between the gate electrode and the source region of the current controlling TFT 108. Thus, the potential given to the pixel electrode of the EL element 109 is determined by the height of the potential of the video signal inputted to the gate electrode of the current controlling TFT 108. Accordingly, the EL  
15 element 109 is controlled by the potential of the video signal and emits light.

When the above operation is repeated and the input of the video signals to the source signal lines (104\_1 to 104\_x) is ended, the first line period (L1) is ended. Note that a combination of a period up to the end of the input of the video signals to the source signal lines (104\_1 to 104\_x) and a horizontal retrace period may be  
20 made one line period. Next, a second line period (L2) is started, the gate signal line 106\_2 is selected by a selection signal, and video signals are sequentially inputted to the source signal lines (104\_1 to 104\_x) similarly to the first line period (L1).

When all the gate signal lines (106\_1 to 106\_y) are selected, all line periods (L1 to Ly) are ended. When all the line periods (L1 to Ly) are ended, one frame  
25 period is ended. In one frame period, every pixel causes a display, and one image is

formed. Note that a combination of all the line periods (L1 to Ly) and a vertical retrace period may be made one frame period.

As described above, the amount of light emission of the EL element is controlled by the potential of the video signal, and a gradation display is carried out  
5 by the control of the amount of light emission.

### [Embodiment 3]

In this embodiment, a detailed description will be given of a method of fabricating a pixel portion and TFTs (n-channel TFT and p-channel TFT) of a driving circuit provided on the periphery of the pixel portion on the same substrate  
10 at the same time.

First, as shown in Fig. 7A, an under film 701 made of an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon nitride oxide film is formed on a substrate 700 made of glass such as barium borosilicate glass or alumino borosilicate glass, typified by #7059 glass or #1737 glass of Corning Inc. For  
15 example, a silicon nitride oxide film 701a fabricated from  $\text{SiH}_4$ ,  $\text{NH}_3$  and  $\text{N}_2\text{O}$  by a plasma CVD method is formed to a thickness of 10 to 200 nm (preferably 50 to 100 nm), and a hydrogenated silicon nitride oxide film 701b similarly fabricated from  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  is formed to a thickness of 50 to 200 nm (preferably 100 to 150 nm) to form a laminate. In this embodiment, although the under film 701 is shown as the  
20 two-layer structure, the film may be formed of a single layer film of the foregoing insulating film or as a laminate structure of more than two layers.

Next, a semiconductor film (amorphous semiconductor film) 702 having a thickness of 20 to 150 nm (preferably 30 to 80 nm) and an amorphous structure is formed by a well-known method such as a plasma CVD method or a sputtering



method. In this embodiment, an amorphous silicon film was formed to a thickness of 55 nm by the plasma CVD method. The semiconductor film having the amorphous structure includes an amorphous semiconductor film and a microcrystalline semiconductor film, and a compound semiconductor film having an amorphous structure, such as an amorphous silicon germanium film, may also be applied. Since the under film 701 and the amorphous silicon film 702 can be formed by the same film forming method, both may be continuously formed. When the under film is not exposed to the air after its formation, it becomes possible to prevent contamination of its surface, and the fluctuation of characteristics of fabricated TFTs and the change of threshold voltage can be decreased (Fig. 7A).

Next, a crystalline semiconductor film is formed by a thermal crystallization method using a catalytic element. In the case where the catalytic element is used, it is desirable to use a technique disclosed in Japanese Patent Laid-Open No. Hei 7-130652 or No. Hei 8-78329.

First, a silicon oxide film having a thickness of 150 nm was formed on the amorphous semiconductor film 702, and patterning was carried out to form masks 703 to 705. The silicon oxide film may be continuously formed together with the amorphous semiconductor film 702, or may be continuously formed together with the under film 701 and the amorphous semiconductor film 702.

Next, a nickel acetate salt solution containing nickel of 10 ppm in terms of weight was coated. By this, a nickel containing layer 706 was formed, and the nickel containing layer 706 was brought into contact with the amorphous semiconductor film 702 only at bottom portions of opening portions 707 and 708 (Fig. 7B).

Next, a heat treatment at 500 to 650°C for 4 to 24 hours, for example, at 570°C for 14 hours was carried out to form a crystalline semiconductor film 709. In

this crystallization process, a portion of the amorphous semiconductor film 702 with which nickel is in contact is first crystallized, and crystallization proceeds in the horizontal direction from that. The crystalline semiconductor film 709 formed in this way is made of an aggregate of rod-like or needle-like crystals, and the  
5    respective crystals grow with certain specific directionality when they are macroscopically seen, so that there is a merit that crystallinity is uniform (Fig. 7B).

Note that in the above two techniques, as a usable catalytic element, in addition to nickel (Ni), an element such as germanium (Ge), iron (Fe), palladium  
10    (Pd), tin (Sn), lead (Pb), cobalt (Co), platinum (Pt), copper (Cu), or gold (Au) may be used.

Next, phosphorus was doped so that regions 710 and 711 added with phosphorus were provided in regions where the crystalline semiconductor film 709 was exposed at the opening portions 707 and 708.

15    In this state, when a heat treatment at 550 to 800°C for 5 to 24 hours, for example, at 600°C for 12 hours was carried out in a nitrogen atmosphere, the regions 710 and 711 where phosphorus was added into the crystalline semiconductor film 709 function as gettering sites, so that it was possible to make the catalytic element remaining in the crystalline semiconductor film 709 segregate  
20    into the regions 710 and 711 added with phosphorus (Fig. 7C).

Then, the masks 703 to 705 and the regions 710 and 711 where phosphorus was added were removed by etching, and patterning was carried out, so that it was possible to obtain island-like semiconductor films 712 to 715 where the concentration of the catalytic element used in the step of crystallization was reduced  
25    to  $1 \times 10^{17}$  atoms/cm<sup>3</sup> or less.

Note that in this embodiment, although crystallization of the amorphous semiconductor film 702 was carried out by using the catalytic element, the present invention is not limited to this method, but a well-known crystallization technique can be used. As the well-known crystallization technique, for example, a heat  
5 crystallization method using an electronic furnace, a laser annealing crystallization method using laser light, and a lamp annealing crystallization method using infrared light can be named as a well-known crystallization method.

In order to fabricate the crystalline semiconductor film by the laser crystallization method, a pulse oscillation type or continuous-wave excimer laser,  
10 YAG laser, or  $\text{YVO}_4$  laser is used. In the case where such laser is used, it is appropriate that there is used a method in which laser light radiated from a laser oscillator is collected by an optical system into a linear beam and is irradiated to the amorphous semiconductor film. Although the condition of crystallization should be properly selected by an operator, in the case where the excimer laser is used, a pulse  
15 oscillation frequency is made 300 Hz, and a laser energy density is made 100 to 400  $\text{mJ}/\text{cm}^2$  (typically 200 to 300  $\text{mJ}/\text{cm}^2$ ). In the case where the YAG laser is used, it is appropriate that the second harmonic is used, a pulse oscillation frequency is made 30 to 300 Hz, and a laser energy density is made 300 to 600  $\text{mJ}/\text{cm}^2$  (for example, 350 to 500  $\text{mJ}/\text{cm}^2$ ). Then, laser light collected into a linear shape with a width of  
20 100 to 1000  $\mu\text{m}$ , for example, 400  $\mu\text{m}$  is irradiated to the whole surface of the substrate, and an overlapping ratio (overlap ratio) of the linear laser light at this time is made 50 to 90%.

Besides, before the step of crystallization, although depending on the hydrogen content of the amorphous semiconductor film, crystallization may be carried out  
25 after a heat treatment at 400 to 500°C for about 1 hour is carried out to make the

hydrogen content 5 atom % or less. When the amorphous semiconductor film is crystallized, since atoms are rearranged and the film becomes dense, the thickness of the fabricated crystalline semiconductor film was decreased by about 1 to 15 % from the initial thickness of the amorphous semiconductor film.

5        The island-like semiconductor layers 712 to 715 are formed to a thickness of 25 to 80 nm (preferably 30 to 60 nm).

Next, a first shape gate insulating film 716 covering the island-like semiconductor layers 712 to 715 is formed. The first shape gate insulating film 716 is formed of an insulating film having a thickness of 40 to 150 nm and containing  
10    silicon by using a plasma CVD method or a sputtering method. In this embodiment, this film is formed of a silicon nitride oxide film having a thickness of 120 nm. Of course, the gate insulating film is not limited to such silicon nitride oxide film, but another insulating film containing silicon may be used as a single layer or a laminate structure. For example, in the case where a silicon oxide film is used, TEOS  
15    (Tetraethyl Orthosilicate) and O<sub>2</sub> are mixed with each other by the plasma CVD method, a reaction pressure is made 40 Pa, a substrate temperature is made 300 to 400°C, and discharge is made at a high frequency (13.56 MHz) power density 0.5 to 0.8 W/cm<sup>2</sup>, so that the film can be formed. Thereafter, the silicon oxide film fabricated in this way is subjected to heat annealing at 400 to 500°C so that  
20    excellent characteristics as the gate insulating film can be obtained (Fig. 7D).

Then, a first conductive film 718 and a second conductive film 719 for forming a gate electrode are formed on the first shape gate insulating film 716. In this embodiment, the first conductive film 718 is formed of Ta (tantalum) and to a thickness of 50 to 100 nm, and the second conductive film 719 is formed of W  
25    (tungsten) and to a thickness of 100 to 300 nm (Fig. 8A).

The Ta film is formed by a sputtering method, and a target of Ta is sputtered by Ar. In this case, when a suitable amount of Xe or Kr is added to Ar, it is possible to relieve internal stress of the Ta film and to prevent peeling of the film. Although the resistivity of a  $\alpha$ -phase Ta film is about  $20\ \mu\Omega\text{cm}$  and can be used as the gate electrode, the resistivity of a  $\beta$ -phase Ta film is about  $180\ \mu\Omega\text{cm}$  and is unsuitable for the gate electrode. In order to form the  $\alpha$ -phase Ta film, if tantalum nitride having crystal structure close to the  $\alpha$  phase of Ta is formed to a thickness of about 10 to 50 nm as an under layer of Ta, the  $\alpha$ -phase Ta film can be easily obtained.

In the case where the W film is formed, the film is formed by the sputtering method using W as a target. In addition to this, the film can also be formed by a thermal CVD method using tungsten hexafluoride ( $\text{WF}_6$ ). In any case, in order to use the film as the gate electrode, it is necessary to lower the resistance, and it is desirable that the resistivity of the W film is made  $20\ \mu\Omega\text{cm}$  or less. Although the resistivity of the W film can be lowered by enlarging crystal grains, in the case where a lot of impurity elements of oxygen or the like exist in W, crystallization is hindered and the resistivity becomes high. From this, in the case of the sputtering method, a W target of purity 99.9999% or 99.99 % is used, and further, the W film is formed while arrangements are thoroughly made to prevent an impurity from mixing from a vapor phase at the film formation, so that a resistivity of 9 to  $20\ \mu\Omega\text{cm}$  can be realized.

Note that in this embodiment, although the first conductive film 718 is made of Ta, and the second conductive film 719 is made of W, the present invention is not particularly limited, and either film may be formed of an element selected from Ta, W, Ti, Mo, Al, and Cu, or an alloy material or a compound material containing the above element as its main ingredient. Besides, a semiconductor film typified by

a polycrystalline silicon film doped with an impurity element such as phosphorus may be used. As examples of combinations other than this embodiment, it is preferable to form the film by a combination in which the first conductive film is formed of tantalum nitride (TaN) and the second conductive film is formed of W, 5 a combination in which the first conductive film is formed of tantalum nitride (TaN) and the second conductive film is formed of Al, or a combination in which the first conductive film is formed of tantalum nitride (TaN) and the second conductive film is formed of Cu.

Next, resist masks 720 to 726 are formed, and a first etching treatment for 10 forming electrodes and wiring lines is carried out. In this embodiment, an ICP (Inductively Coupled Plasma) etching method is used, in which  $\text{CF}_4$  and  $\text{Cl}_2$  are mixed in an etching gas, and an RF (13.56 MHz) power of 500 W is applied to a coil type electrode under a pressure of 1 Pa to generate plasma. An RF (13.56 MHz) power of 100 W is also applied to the side of the substrate (sample stage) and 15 substantially negative self bias voltage is applied. In the case where  $\text{CF}_4$  and  $\text{Cl}_2$  are mixed with each other, both the W film and the Ta film are etched to the same degree.

Under the above etching condition, by making the shapes of the resist masks suitable, end portions of a first conductive layer and a second conductive layer 20 become taper-shaped by the effect of the bias voltage applied to the substrate side. The angle of the taper portion becomes 15 to 45°. In order to carry out the etching without leaving a residue on the gate insulating film, it is appropriate that an etching time is increased at a rate of about 10 to 20 %. Since the selection ratio of the silicon nitride oxide film to the W film is 2 to 4 (typically 3), a surface on which 25 the silicon nitride oxide film is exposed is etched by an over etching treatment by

about 20 to 50 nm. In this way, first shape conductive layers 727 to 733 made of first conductive layers and second conductive layers (first shape first conductive layers 722a to 733a and first shape second conductive layers 722b to 733b) are formed by the first etching treatment. Reference numeral 750 designates a second shape gate  
5 insulating film, and regions which are not covered with the first shape conductive layers 727 to 733 are etched by about 20 to 50 nm so that thinned regions are formed (Fig. 8B).

Then, a first doping treatment is carried out to add an impurity element to give an n type. Doping may be carried out by an ion doping method or an ion injecting  
10 method. The condition of the ion doping method is that a dosage is  $1 \times 10^{13}$  to  $5 \times 10^{14}$  atoms/cm<sup>2</sup>, and an acceleration voltage is 60 to 100 keV. As the impurity element to give the n type, although an element belonging to group 15, typically phosphorus (P) or arsenic (As) is used, phosphorus is used here. In this case, The first shape conductive layers 728, 729, 731, and 733 become masks to the impurity  
15 element to give the n type, and first impurity regions 734 to 737 are formed in a self aligning manner. The impurity element to give the n type in the concentration range of  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup> is added to the first impurity regions 734 to 737 (Fig. 8B).

Next, as shown in Fig. 8C, a second etching treatment is carried out. The ICP  
20 etching method is similarly used, in which CF<sub>4</sub>, Cl<sub>2</sub> and O<sub>2</sub> are mixed in an etching gas, and an RF power (13.56 MHz) of 500 W is applied to a coil type electrode under a pressure of 1 Pa to generate plasma. An RF (13.56 MHz) power of 50 W is applied to the side of the substrate (sample stage) and a low self bias voltage as compared with the first etching treatment is applied. The W film is anisotropically  
25 etched under the condition like this, and the Ta film as the first conductive layers

is anisotropically etched at an etching rate lower than that to form second shape  
conductive layers 738 to 744 (second shape first conductive layers 738a to 744a and  
second shape second conductive layers 738b to 744b). Reference numeral 745  
designates a third shape gate insulating film, and regions which are not covered with  
5 the second shape conductive layers 738 to 744 are further etched by about 20 to 50  
nm so that thinned regions are formed.

An etching reaction of the W film or the Ta film by the mixture gas of  $\text{CF}_4$  and  
 $\text{Cl}_2$  can be guessed from a generated radical or ion species and the vapor pressure of  
a reaction product. When the vapor pressures of fluoride and chloride of W and Ta  
10 are compared with each other,  $\text{WF}_6$  as fluoride of W is extremely high, and other  
 $\text{WCl}_5$ ,  $\text{TaF}_5$ , and  $\text{TaCl}_5$  have almost equal vapor pressures. Thus, in the mixture gas  
of  $\text{CF}_4$  and  $\text{Cl}_2$ , both the W film and the Ta film are etched. However, when a  
suitable amount of  $\text{O}_2$  is added to this mixture gas,  $\text{CF}_4$  and  $\text{O}_2$  react with each other  
to form CO and F, and a large number of F radicals or F ions are generated. As a  
15 result, an etching rate of the W film having the high vapor pressure of fluoride is  
increased. On the other hand, with respect to Ta, even if F is increased, an increase  
of the etching rate is relatively small. Besides, since Ta is easily oxidized as compared  
with W, the surface of Ta is oxidized by addition of  $\text{O}_2$ . Since the oxide of Ta does  
not react with fluorine or chlorine, the etching rate of the Ta film is further  
20 decreased. Accordingly, it becomes possible to make a difference between the  
etching rates of the W film and the Ta film, and it becomes possible to make the  
etching rate of the W film higher than that of the Ta film.

Then, as shown in Fig. 8D, a second doping treatment is carried out. In this  
case, a dosage is made lower than that of the first doping treatment and under the  
25 condition of a high acceleration voltage, an impurity element to give the n type is



doped. For example, an acceleration voltage is made 70 to 120 keV, and the treatment is carried out at a dosage of  $1 \times 10^{13}$  atoms/cm<sup>2</sup>, so that new impurity regions are formed inside of the first impurity regions formed into the island-like semiconductor layers in Fig. 8B. Doping is carried out in such a manner that the second shape conductive layers 739, 740, 742 and 744 are used as masks to the impurity element and the impurity element is added also to the regions under the second conductive layers 739a, 740a, 742a and 744a. In this way, third impurity regions 746b to 749b overlapping with the second conductive layers 739a, 740a, 742a and 744a, and second impurity regions 746a to 749a between the first impurity regions and the third impurity regions are formed. The impurity element to give the n type is made to have a concentration of  $1 \times 10^{17}$  to  $1 \times 10^{19}$  atoms/cm<sup>3</sup> in the second impurity regions, and a concentration of  $1 \times 10^{16}$  to  $1 \times 10^{18}$  atoms/cm<sup>3</sup> in the third impurity regions.

Then, as shown in Fig. 9A, fourth impurity regions 753a and 754a, fifth impurity regions 753b and 754b, sixth impurity regions 753c and 754c having a conductivity type opposite to the former conductivity type are formed in the island-like semiconductor layers 713 and 715 forming p-channel TFTs. The second conductive layers 740 and 744 are used as masks to an impurity element, and the impurity regions are formed in a self aligning manner. At this time, the whole surfaces of the island-like semiconductor layers 712 and 714 forming n-channel TFTs are covered with resist masks 751 and 752. Phosphorus is added to the impurity regions 753a, 753b and 753c at different concentrations, respectively, and phosphorus is added to the impurity regions 754a, 754b and 754c at different concentrations, respectively. The regions are formed by an ion doping method using diborane (B<sub>2</sub>H<sub>6</sub>) and the impurity concentration is made  $2 \times 10^{20}$  to  $2 \times 10^{21}$

atoms/cm<sup>3</sup> in any of the regions.

By the steps up to this, the impurity regions are formed in the respective island-like semiconductor regions. The second shape second conductive layers 739, 740, 742, and 744 overlapping with the island-like semiconductor layers function  
5 as gate electrodes. The layer 741 functions as an island-like source signal line, the layer 738 functions as a wiring line, and the layer 743 functions as a gate signal line.

A step of activating the impurity elements added in the respective island-like semiconductor layers for the purpose of controlling the conductivity type in this  
10 way, as shown in Fig. 9B, is carried out. This step is carried out by a thermal annealing method using a furnace annealing oven. In addition, a laser annealing method or a rapid thermal annealing method (RTA method) can be applied. The thermal annealing method is carried out in a nitrogen atmosphere having an oxygen content of 1 ppm or less, preferably 0.1 ppm or less and at 400 to 700°C, typically  
15 500 to 600°C. In this embodiment, a heat treatment at 500°C for 4 hours is carried out. However, in the case where a wiring material used for the second conductive layers 738 to 744 is weak to heat, it is preferable that the activation is carried out after an interlayer insulating film (containing silicon as its main ingredient) is formed to protect the wiring line or the like.

20 Further, a heat treatment at 300 to 450°C for 1 to 12 hours is carried out in an atmosphere containing hydrogen of 3 to 100 %, so that a step of hydrogenating the island-like semiconductor layers is carried out. This step is a step of terminating dangling bonds in the semiconductor layer by thermally excited hydrogen. As another means for hydrogenation, plasma hydrogenation (using hydrogen excited  
25 by plasma) may be carried out.

Next, a first interlayer insulating film 755 having a thickness of 100 to 200 nm is formed from a silicon nitride oxide film. A second interlayer insulating film 756 made of an organic insulator material is formed thereon. Next, an etching step for forming contact holes is carried out.

5        Then, in a driving circuit 806, source wiring lines 757 and 758 in contact with source regions of the island-like semiconductor layers and drain wiring lines 759 and 760 in contact with drain regions are formed. In a pixel portion 807, a connection electrode 761, source wiring lines 761 and 762, and drain wiring lines 763 and 764 are formed (Fig. 9C). By this connection electrode 761, the island-like source signal  
10   line 741 is electrically connected to the switching TFT 804.

In the manner as described above, the driving circuit 806 including an n-channel TFT 801 and a p-channel TFT 802 and the pixel portion 807 including a switching TFT 804 and a current controlling TFT 805 can be formed on the same  
15   substrate for convenience.

The n-channel TFT 801 of the driving circuit 806 includes a channel forming region 788, the third impurity region 746b (GOLD region) overlapping with the second shape second conductive layer 739 forming the gate electrode, the second impurity region 746a (LDD region) in contact with the third impurity region 746b,  
20   and the first impurity region 734 functioning as a source region or a drain region. The p-channel TFT 802 includes a channel forming region 789, the fourth impurity region 753c overlapping with the second conductive layer 740 forming the gate electrode, the fifth impurity region 753b in contact with the fourth impurity region 753c, and the sixth impurity region 753a functioning as a source region or a drain  
25   region.

The switching TFT 804 of the pixel portion includes a channel forming region 790, the third impurity region 748b (GOLD region) overlapping with the second shape second conductive layer 742 forming the gate electrode, the second impurity region 748a (LDD region) in contact with the third impurity region 748b, and the  
5 first impurity region 736 functioning as a source region or a drain region. The current controlling TFT 805 includes a channel forming region 791, the fourth impurity region 754c overlapping with the second shape second conductive layer 744 forming the gate electrode, the fifth impurity region 754b in contact with the fourth impurity region 754c, and the sixth impurity region 754a functioning as a  
10 source region or a drain region.

Next, as shown in Fig. 10A, a first passivation film 766 is formed to a thickness of 50 to 500 nm (typically 200 to 300 nm). In this embodiment, as the first passivation film 766, a silicon nitride oxide film having a thickness of 300 nm is used. A silicon nitride film may be substituted for this. Note that it is effective to  
15 carry out a plasma treatment using a gas containing hydrogen, such as  $H_2$  or  $NH_3$ , before the silicon nitride oxide film is formed. Hydrogen excited by this pretreatment is supplied to the second interlayer insulating film 756, and the film quality of the first passivation film 766 is improved by carrying out a heat treatment. At the same time, since hydrogen added to the second interlayer insulating film 756  
20 is diffused to the lower layer side, the active layer can be effectively hydrogenated.

Next, a third interlayer insulating film 767 made of an organic resin is formed. As the organic resin, polyimide, polyamide, acryl, BCB (benzocyclobutene) or the like can be used. Especially, since the third interlayer insulating film 767 has rather  
25 the meaning of flattening, acryl excellent in flatness is desirable. In this

embodiment, an acryl film is formed to such a thickness that stepped portions formed by the TFTs can be adequately flattened. It is appropriate that the thickness is preferably made 1 to 5  $\mu\text{m}$  (more preferably 2 to 4  $\mu\text{m}$ ) (Fig. 10A).

Next, a contact hole reaching the drain wiring line 764 is formed in the third  
5 interlayer insulating film 767 and the first passivation film 766, and a pixel electrode 768 is formed. In this embodiment, an indium-tin oxide (ITO) film is formed to a thickness of 110 nm, and patterning is carried out to form the pixel electrode 768. Besides, a transparent electrode in which zinc oxide (ZnO) of 2 to 20% is mixed with indium oxide may be used. This pixel electrode 768 corresponds to an anode  
10 of an EL element.

Next, an organic resin film is formed on the pixel electrode 768 and the third interlayer insulating film 767, and the organic resin film is patterned, so that a bank 769 and a flattening portion 770 are formed. In this embodiment, as the organic resin film, an acryl film or a polyimide film having a thickness of 1 to 2  $\mu\text{m}$  was  
15 used.

The bank 769 is formed into a stripe shape between a pixel and a pixel to separate light-emitting layers or EL layers of adjacent pixels. In this embodiment, although the bank 769 is formed along the source wiring line 741, it may be formed along the gate wiring line 743. Note that a pigment or like may be added to the resin  
20 material forming the bank 769 so that the bank 769 is used as a light shielding film.

The flattening portion 770 is provided on a portion where the pixel electrode 768 is connected with the drain wiring line 764 of the current controlling TFT 805. Since there is a case where the connection of the pixel electrode 768 with the drain  
25 wiring line 764 is cut off by a stepped portion of the contact hole, it is desirable to

make flattening by providing the flattening portion 770 in order to prevent poor light emission of an EL layer 771 formed later. Note that the bank 769 and the flattening portion 770 may not be formed to the same thickness, and can be suitably set in accordance with the thickness of the later formed EL layer 771.

5       Next, the EL layer 771 and a cathode (MgAg electrode) 722 are continuously formed by using a vacuum evaporation method without exposing to the air. Note that it is appropriate that the thickness of the EL layer 771 is made 80 to 200 nm (typically 100 to 120 nm), and the thickness of the cathode 772 is made 180 to 300 nm (typically 200 to 250 nm). Note that in this embodiment, although only one  
10       pixel is shown, at this time, an EL layer emitting red light, an EL layer emitting green light, and an EL layer emitting blue light are formed at the same time.

          In this step, the EL layer 771 is sequentially formed for a pixel corresponding to red, a pixel corresponding to green, and a pixel corresponding to blue. However, since the EL layer 771 has poor resistance against a solution, the layer must be  
15       formed individually for respective colors without using a photolithography technique. Then, it is preferable that portions other than a desired pixel are concealed by using metal masks, and the EL layer 771 is selectively formed on only a necessary portion.

          That is, first, a mask for concealing all portion other than the pixel  
20       corresponding to red is set, and the EL layer emitting red light is selectively formed using the mask. Next, a mask for concealing all portion other than the pixel corresponding to green is set, and the EL layer emitting green light is selectively formed using the mask. Next, similarly, a mask for concealing all portion other than the pixel corresponding to blue is set, and the EL layer emitting blue light is  
25       selectively formed using the mask. Note that here, although the recitation is such

that different masks are used for the respective pixels, the same mask may be commonly used. Besides, it is preferable that the treatment is carried out without breaking a vacuum until the EL layers are formed for all pixels.

Note that in this embodiment, although the EL layer 771 is made to have a single layer structure of only a light-emitting layer, the EL layer may include a hole transporting layer, a hole injecting layer, an electron transporting layer, an electron injecting layer, or the like in addition to the light-emitting layer. Like this, various examples have been already reported with respect to the combination, and any structure of those may be used. As the EL layer 771, a well-known material can be used. As the well-known material, in view of EL driving voltage, it is preferable to use an organic material.

Next, the cathode 772 is formed. Although this embodiment shows an example in which a MgAg electrode is used as a cathode of an EL element, another well-known material can be used.

In this way, an active matrix substrate having a structure as shown in Fig. 10B is completed. Note that it is effective that after the bank 769 and the flattening portion 770 are formed, steps up to the formation of the cathode 772 are continuously carried out by using a thin film forming apparatus of a multichamber system (or an inline system) without opening to the air.

In this embodiment, the switching TFT 804 is made to have a double gate structure, and by making the double gate structure, there is obtained a structure in which two TFTs are substantially connected in series with each other, and there is a merit that an off current value can be decreased. Although this embodiment adopts the double gate structure, a single gate structure may be adopted, or a triple gate structure or a multigate structure having more gates may be adopted.

Note that actually, when the state of Fig. 10B is completed, it is preferable to make packaging (sealing) by a protective film (lamine film, ultraviolet ray curing resin film, etc.), which has high airtightness and hardly causes degassing, or a translucent sealing member so as to prevent exposure to the outer air. At that time,  
5 if the inside of the sealing member is made an inert atmosphere or a hygroscopic material (for example, barium oxide) is disposed in the inside, the reliability of the EL element is improved.

After the airtightness is raised by the treatment such as packaging, a connector (Flexible Printed Circuit: FPC) for connecting a terminal extended from the  
10 element or the circuit formed on the substrate to an external signal terminal is attached so that a product is completed.

#### [Embodiment 4]

In this embodiment, an example in which a light-emitting device is fabricated by using the present invention will be described. Fig. 11A is a top view of the light-  
15 emitting device of the present invention, and Fig. 11B is a sectional view thereof.

In Fig. 11A, reference numeral 4001 designates a substrate; 4002, a pixel portion; 4003, a source signal line driving circuit; and 4004, a gate signal line driving circuit. The respective driving circuits lead to an FPC (Flexible Printed Circuit) 4006 through a wiring line 4005 and are connected to an external instrument.

20 At this time, a first seal member 4101, a cover member 4102, a filler member 4103, and a second seal member 4104 are provided so as to surround the pixel portion 4002, the source signal line driving circuit 4003, and the gate signal line driving circuit 4004.

Fig. 11B is a sectional view taken along line A-A' of Fig. 11A, and a driving



TFT (here, an n-channel TFT and a p-channel TFT are shown) 4201 included in the source signal line driving circuit 4003 and a current controlling TFT (TFT for controlling current to an EL element) 4202 included in the pixel portion 4002 are formed on the substrate 4001. Note that in Fig. 11B, a switching TFT is not shown  
5 for simplification of the explanation.

In this embodiment, the driving TFT 4201 and the current controlling TFT 4202 are formed by using a well-known fabricating method. Besides, a holding capacitance (not shown) connected to a gate electrode of the current controlling TFT 4202 is provided in the pixel portion 4002.

10 An interlayer insulating film (flattening film) 4301 made of a resin material is formed on the driving TFT 4201 and the switching TFT 4202, and a pixel electrode (anode) 4302 electrically connected to a drain region of the pixel TFT 4202 is formed thereon. As the pixel electrode 4302, a transparent conductive film having a large work function is used. As the transparent conductive film, a compound of  
15 indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, or indium oxide can be used. The transparent conductive film added with gallium may be used.

Then, an insulating film 4303 is formed on the pixel electrode 4302, and an opening portion is formed in the insulating film 4303 on the pixel electrode 4302.  
20 At this opening portion, an EL (electroluminescence) layer 4304 is formed on the pixel electrode 4302. As the EL layer 4304, a well-known organic EL material or an inorganic EL material can be used. Although the organic EL material includes a low molecular (monomer) material and a high molecular (polymer) material, either may be used.

25 As a method of forming the EL layer 4304, a well-known evaporation

technique or coating technique may be used. The structure of the EL layer may be made a laminate structure by freely combining a hole injecting layer, a hole transporting layer, a light-emitting layer, an electron transporting layer, and an electron injecting layer or a single layer structure.

- 5        A cathode 4305 made of a conductive film (typically, a conductive film containing aluminum, copper or silver as its main ingredient, or a laminate film of those and another conductive film) having a light shielding property is formed on the EL layer 4304. It is desirable that moisture and oxygen existing at the interface between the cathode 4305 and the EL layer 4304 are removed to the utmost degree.
- 10      Accordingly, it is necessary to make such contrivance that both are continuously formed in vacuum, or the EL layer 4304 is formed in a nitrogen or rare gas atmosphere, and the cathode 4305 is formed while the layer is not put into contact with oxygen and moisture. In this embodiment, a film forming apparatus of a multichamber system (cluster tool system) is used so that the film formation as
- 15      described above is made possible.

The cathode 4305 is electrically connected to the wiring line 4005 in a region designated by 4306. The wiring line 4005 is a wiring line for giving a predetermined voltage to the cathode 4305, and is electrically connected to the FPC 4006 through an anisotropic conductive film 4307.

- 20        In the manner as described above, an EL element constituted by the pixel electrode (anode) 4302, the EL layer 4304, and the cathode 4305 is formed. This EL element is surrounded by the cover member 4102 bonded to the substrate 4001 by the first seal member 4101 and the second seal member 4104 and is sealed by the filler member 4103.

- 25        As the cover member 4102, a glass member, a metal member (typically a

stainless member), a ceramic member, or a plastic member (including a plastic film as well) can be used. As the plastic member, an FRP (Fiberglass-Reinforced Plastics) plate, a PVF (polyvinyl fluoride) film, a Mylar film, a polyester film, or an acrylic resin film can be used. Besides, a sheet having a structure in which an aluminum foil  
5 is sandwiched between PVF films or Mylar films can also be used.

However, in the case where the radiation of light from the EL element is directed toward the side of the cover member, the cover member must be transparent. In that case, a transparent material such as a glass plate, a plastic plate, a polyester film or an acryl film is used.

10 As the filler member 4103, an ultraviolet ray curing resin or a thermosetting resin can be used, and PVC (polyvinyl chloride), acryl, polyimide, epoxy resin, silicone resin, PVB (polyvinyl butyral) or EVA (ethylene-vinyl acetate) can be used. If a hygroscopic material (preferably barium oxide) or a material capable of adsorbing oxygen is provided in the inside of this filler member 4103, deterioration  
15 of the EL element can be suppressed.

A space may be included in the filler member 4103. At this time, if the spacer is formed of barium oxide, it is possible to make the spacer itself have a hygroscopic property. Besides, in the case where the spacer is provided, as a buffer layer for relieving stress from the spacer, it is also effective to provide a resin film on the  
20 cathode 4305.

The wiring line 4005 is electrically connected to the FPC 4006 through the anisotropic conductive film 4307. The wiring line 4005 connected to the pixel portion 4002, the source signal line driving circuit 4003, and the gate signal line driving circuit 4004 are electrically connected to an outside instrument through the  
25 FPC 4006.

Besides, in this embodiment, a second seal member 4104 is provided so as to cover an exposed portion of the first seal member 4101 and a part of the FPC 4006, and a structure to thoroughly shut off the EL element from the outer air is adopted.

## 5 [Embodiment 5]

In this embodiment, examples of pixel structures which can be used for the pixel portion of the light-emitting device set forth in the embodiments 1 to 4 are shown in Figs. 12A to 12C. In this embodiment, reference numeral 4601 designates a source signal line; 4602, a switching TFT; 4603, a gate signal line; 4604, a current  
10 controlling TFT; 4605, a capacitor; 4606 and 4608, power supply lines; and 4607, an EL element.

Fig. 12A is a circuit diagram in a case where two pixels including the same gate signal line own the power supply line 4606 jointly. That is, the feature is that the two pixels are formed to be axially symmetrical with respect to the power supply line  
15 4606. In this case, since the number of power supply lines can be decreased, the pixel portion can be made highly fine.

Fig. 12B is a circuit diagram in a case where the power supply line 4608 is provided in parallel with the gate signal line 4603. Note that although Fig. 12B shows the structure in which the power supply line 4608 does not overlap with the  
20 gate signal line 4603, if both are wiring lines formed in different layers, they can also be formed so as to overlap with each other through an insulating film. In this case, since an occupied area can be jointly owned by the power supply line 4608 and the gate signal line 4603, the pixel portion can be made highly fine.

Fig. 12C has a feature that the power supply line 4608 is provided in parallel

with gate signal lines 4603 (4603a, 4603b) similarly to the structure of Fig. 12B, and further, two pixels are formed to be axially symmetrical with respect to the power supply line 4608. It is also effective that the power supply line 4608 is provided to overlap with one of the gate signal lines 4603a and 4603b. In this case, since the  
5 number of power supply lines can be decreased, the pixel portion can be further made highly fine.

#### [Embodiment 6]

In this embodiment, a detailed circuit structure of a source signal line driving circuit of a light-emitting device of the present invention will be described with  
10 reference to Fig. 13.

Reference numeral 1301 designates a shift register; 1302, a level shift; 1303, a sampling circuit; 1304, an analog switch; and 1305, a video signal.

A clock signal (CLK) as a panel control signal, and a start pulse signal (SP) are inputted to the shift register 1301. A sampling signal for sampling a video signal is  
15 outputted from the shift register 1301. The outputted sampling signal is inputted to the level shift 1302.

The amplitude of the potential of the clock signal inputted to the level shift 1302 is made large. Fig. 14A is an equivalent circuit diagram of the level shift 1302. Reference characters  $V_{in}$  and  $V_{inb}$  designate input terminals, and  $V_{inb}$  means that  
20 a signal having a potential equal to an inversion of a potential of a signal inputted to  $V_{in}$  is inputted. Reference character  $V_{ddh}$  designates a voltage of a power source at a high voltage side, and  $V_{ss}$  designates a voltage of a power source at a low voltage side. Reference character  $V_{outb}$  designates an output terminal, and the level shift 1302 is designed such that a signal obtained by boosting and inverting a signal

inputted to  $V_{in}$  is outputted from  $V_{outb}$ . That is, when  $H_i$  is inputted to  $V_{in}$ , a signal corresponding to  $V_{ss}$  is outputted from  $V_{outb}$ , and when  $L_o$  is inputted, a signal corresponding to  $V_{ddh}$  is outputted from  $V_{out}$ .

Note that in this embodiment, although the level shift having the structure shown in Fig. 14A is used, the present invention is not limited to this. In the light-emitting device of the present invention, a level shift having a well-known structure can be used.

The sampling signal outputted from the level shift 1302 is inputted to the sampling circuit 1303. At the same time, the video signal is inputted to the sampling circuit 1303 through the video signal line 1305.

The sampling circuit 1303 includes the analog switch 1304. Fig. 14B is an equivalent circuit diagram of the analog switch 1304 used in this embodiment. A voltage of the sampling signal inputted to the sampling circuit 1303 is applied to a gate electrode of a TFT constituting the analog switch 1304 of the sampling circuit 1303. By this, a channel is formed in the TFT constituting the analog switch 1304, and a current flows from a source to a drain. Thus, the video signal is sampled and is supplied to a source of a pixel TFT through a source signal line ( $S_1$ ,  $S_2$ ).

Note that although the analog switch having the structure shown in Fig. 14B is used in this embodiment, the present invention is not limited to this. In the light-emitting device of the present invention, an analog switch having a well-known structure can be used. Besides, in Fig. 13, although only two signal lines  $S_1$  and  $S_2$  are shown for simplification of the explanation, the number of source signal lines of this embodiment is not limited to this.

Note that this embodiment can be carried out in combination with all embodiments of the present specification.

[Embodiment 7]

In this embodiment, an upper view of a pixel of a light-emitting device of the present invention is shown in Fig. 15 as an example.

Reference numeral 1501 designates a switching TFT, which includes a gate  
5 electrode 1501\_1 and an active layer 1501\_2. Reference numeral 1502 designates  
a current controlling TFT, which includes an active layer 1502\_2 and a gate  
electrode 1502\_2 as a part of a wiring line 1509. Note that in this embodiment,  
although the switching TFT 1501 is made to have a double gate structure, and the  
current controlling TFT 1502 is made to have a single gate structure, the present  
10 invention is not limited to this constitution. The switching TFT 1501 and the  
current controlling TFT 1502 may have a single gate structure, or may have a  
multigate structure such as a double gate structure or a triple gate structure.

Reference numeral 1503 designates a source signal line; 1504, a power supply  
line; and 1505, a gate signal line. The source signal line 1503 is connected to the  
15 active layer 1501\_2 of the switching TFT 1501 through a contact hole. The power  
supply line 1504 is connected to a source region of the active layer 1502\_2 of the  
current controlling TFT 1502 through a contact hole. The gate signal line 1505 is  
connected to the gate electrode 1501\_1 of the switching TFT 1501.

The wiring line 1509 including the gate electrode 1502\_1 of the current  
20 controlling TFT 1502 overlaps with the power supply line 1504 through an  
insulating film in a region indicated by 1511. At this time, a holding capacitance  
(capacitor) is formed in the region indicated by 1511. The holding capacitance 1511  
is formed of a semiconductor film 1510 electrically connected to the power supply  
line 1504, an insulating film (not shown) of the same layer as the gate insulating  
25 film, and the wiring line 1509. A capacitance formed of the wiring line 1509, the

same layer (not shown) as the first interlayer insulating film, and the power supply line 1504 can also be used as a holding capacitance. This holding capacitance 1511 functions as a capacitor for holding voltage applied to the gate electrode 1502\_1 of the current controlling TFT 1502. The source region of the current controlling TFT 1502 is connected to the power supply line (power source line) 1504 and a constant voltage is always applied.

A first passivation film (not shown) is provided on the switching TFT 1501 and the current controlling TFT 1502, and a flattening film (third interlayer insulating film) (not shown) made of a resin insulating film is formed thereon. It is very important to flatten a stepped portion due to a TFT by using the flattening film. Since a later formed EL layer (not shown) is very thin, there is a case where poor light emission occurs due to the existence of the stepped portion. Accordingly, it is desirable to make flattening before a pixel electrode 1507 is formed so that the EL layer can be formed on the flattest possible surface.

Reference numeral 1507 designates the pixel electrode (a cathode of an EL element) made of a conductive film having high reflectivity, and is electrically connected to the drain region of the current controlling TFT 1502 through a contact hole provided in the first passivation film and the flattening film. As the pixel electrode 1507, it is desirable to use a low resistance conductive film such as an aluminum alloy film, a copper alloy film or a silver alloy film, or a laminate film of those. Of course, a laminate structure with another conductive film may be adopted.

Next, an organic resin film is formed on the pixel electrode 1507 and the flattening film, and the organic resin film is patterned, so that a bank 1506 is formed. The bank 1506 is provided to separate light-emitting layers or EL layers of



adjacent pixels. The light-emitting layer (not shown) is formed in a groove (corresponding to a pixel) formed by the bank 1506. Note that in Fig. 15, although the bank is partially omitted in order to clarify the position of the holding capacitance 1511, it is provided between pixels so as to cover part of the power supply line 1503 and the source signal line 1504. Besides, although only two pixels are shown here, light-emitting layers corresponding to the respective colors of R (red), G (green) and B (blue) may be individually formed. As an organic EL material used for the light-emitting layer, a  $\pi$ -conjugated polymer material is used. As a typical polymer material, polyparaphenylene vinylene (PPV), polyvinylcarbazole (PVK), polyfluorene or the like is named.

Although there are various types as the PPV organic EL material, for example, a material as disclosed in [H. Shenk, H. Becker, O. Gelsen, E. Kluge, W. Kreuder, and H. Spreitzer, "Polymers for Light-emitting Diodes", Euro Display, Proceedings, 1999, p. 33-37] or Japanese Patent Laid-Open No. Hei 10-92576 may be used.

Although this embodiment shows the example in which the polymer material is used as the light-emitting layer, a low molecular organic EL material may be used. Besides, as a charge transporting layer or a charge injecting layer, an inorganic material such as silicon carbide can also be used. As the organic EL material or inorganic material, a well-known material can be used.

This embodiment adopts the EL layer of a laminate structure in which a hole injecting layer (not shown) made of PEDOT (polythiophene) or PANi (polyaniline) is provided on the light-emitting layer. An anode (not shown) made of a transparent conductive film is provided on the hole injecting layer. In the case of this embodiment, since light generated in the light-emitting layer is radiated toward the upper surface side (toward the upper portion of the TFT), the anode must be

translucent. Although a compound of indium oxide and tin oxide or a compound of indium oxide and zinc oxide can be used as the transparent conductive film, since the film is formed after the light-emitting layer and the hole injecting layer having low heat resistance are formed, it is desirable to use a material by which the film can  
5 be formed at the lowest possible temperature.

At the point of time when the anode is formed, the EL element is completed. Note that the EL element here indicates a capacitor formed of the pixel electrode (cathode) 1507, the light-emitting layer, the hole injecting layer and the anode. As shown in Fig. 15, since the pixel electrode 1507 is almost coincident with the area  
10 of a pixel, the whole pixel functions as the EL element. Thus, a use coefficient of light emission is very high, and a bright image display becomes possible.

As described above, the EL display panel of the present invention includes the pixel portion made of the pixel having the structure as shown in Fig. 15, and includes the switching TFT having an adequately low off current value and the  
15 current controlling TFT proof against hot carrier injection. Accordingly, it is possible to obtain the EL display panel having high reliability and enabling an excellent image display.

Note that the structure of this embodiment can be freely combined with the embodiments 1, 2, 6 and 8 and can be carried out.

## 20 [Embodiment 8]

In this embodiment, an example of a film forming apparatus used when an EL layer is formed in the above respective embodiments will be described.

The film forming apparatus of this embodiment will be described with reference to Fig. 19. In Fig. 19, reference numeral 1101 designates a conveying

chamber (A), and the conveying chamber (A) 1101 is provided with a conveying chamber mechanism (A) 1102, in which a substrate 1103 is conveyed. The conveying chamber (A) 1101 is made to have a reduced pressure atmosphere, and is shut off from respective processing chambers by gates. Delivery of the substrate  
5 to the respective processing chambers is performed by the conveying chamber mechanism (A) when the gate is opened. In order to decrease the pressure in the conveying chamber (A) 1101, although an exhaust pump such as an oil rotary pump, a mechanical booster turbo pump, a turbo molecular pump, or a cryopump can be used, the cryopump effective in removing moisture is preferable.

10 In the film forming apparatus of Fig. 19, an exhaust port 1104 is provided at a side of the conveying chamber (A) 1101, and the exhaust pump is provided under that. When such structure is adopted, there is a merit that the maintenance of the exhaust pump becomes easy.

Hereinafter, the respective processing chambers will be described. Note that  
15 since the conveying chamber (A) 1101 comes to have a reduced atmosphere, all processing chambers directly coupled with the conveying chamber (A) 1101 are provided with exhaust pumps (not shown). As the exhaust pump, a mechanical booster pump, a turbo molecular pump, or a cryopump is used.

First, reference numeral 1105 designates a stock chamber in which setting of  
20 the substrate is carried out and which is also called a load lock chamber. The stock chamber 1105 is shut off from the conveying chamber (A) 1101 by a gate 1100a, and a carrier (not shown) on which the substrate 1103 is set is disposed here. Note that the stock chamber 1105 may be divided into a portion for use in carrying a substrate in and a portion for use in carrying a substrate out. Besides, the stock  
25 chamber 1105 is provided with the foregoing exhaust pump and a purge line for

introducing a high purity nitrogen gas or rare gas.

In this embodiment, the substrate 1103 is set on the carrier while its element formation surface is made to face downward. This is for facilitating a face down system (also called a deposit up system) when vapor phase film formation (film  
5 formation by sputter or evaporation) is later carried out. The face down system is a system in which film formation is carried out in a state where an element formation surface of a substrate faces downward, and according to this system, adhesion of dust or the like can be suppressed.

Next, reference numeral 1106 designates a conveying chamber (B) which is  
10 coupled with the stock chamber 1105 through a gate 1100b and includes a conveying chamber mechanism (B) 1107. Reference numeral 1108 designates a baking chamber (bake chamber) which is coupled with the conveying chamber (B) 1106 through a gate 1100d. The baking chamber 1108 includes a mechanism for inverting the top and bottom of the surface of the substrate. That is, the substrate  
15 conveyed in the face down system is once changed to the face up system here. This is for enabling a next processing in a spin coater 1109 to be carried out in the face up system. On the contrary, the substrate which has been subjected to the processing in the spin coater 1109 is again returned to the baking chamber 1108 and is baked, and the top and bottom is again inverted to the face down system, and the  
20 substrate is returned to the stock chamber 1105.

The film formation chamber 1109 provided with the spin coater is coupled with the conveying chamber (B) 1106 through a gate 1100c. The film formation chamber 1109 provided with the spin coater is a film formation chamber in which a solution containing an EL material is coated on the substrate so that a film  
25 containing the EL material is formed, and in this embodiment, a film of a high

molecular (polymer) organic EL material is formed in the film formation chamber 1109 provided with the spin coater. Note that the EL material to be formed into a film includes one used for not only a light-emitting layer but also a charge injecting layer or a charge transporting layer. Besides, any well-known high molecular organic  
5 EL material may be used.

As a typical organic EL material which becomes the light-emitting layer, a PPV (polyparaphenylene vinylene) derivative, a PVK (polyvinylcarbazole) derivative, or a polyfluorene derivative is named. This is also called a  $\pi$ -conjugated polymer. As the charge injecting layer, PEDOT (polythiophene) or PANi (polyaniline) is  
10 named.

Note that in this embodiment, although the film formation chamber using the spin coater is shown, it is not necessary to make limitation to the spin coater, but the film formation chamber may use a dispenser, printing, or ink jet instead of the spin coater. Further, as shown in Fig. 19, a pre-processing chamber 1110, a gas  
15 phase film formation chamber 1111, a sealing chamber 1112, an ultraviolet light irradiation mechanism 1113, a delivery chamber 1114, a conveying chamber mechanism (c) 1115 and gates 1100f, 1100e and 1100g can be equipped.

Besides, the film forming apparatus of this embodiment can be used when the EL layer is formed in the structure in which any structures of the embodiments 1 to  
20 7 are freely combined.

#### [Embodiment 9]

In this embodiment, in a light-emitting device using an organic EL material in which emission brightness of red, blue and green are different, W/L of a current controlling TFT of a pixel for displaying a color with low emission brightness is

made larger than W/L of a current controlling TFT of a pixel for displaying a color with relatively high emission brightness. By the above structure, a drain current of the current controlling TFT of the pixel for displaying the color with the low emission brightness is made higher than a drain current of the current controlling  
5 TFT of the pixel for displaying the color with the relatively high emission brightness.

Thus, in the light-emitting device using the organic EL material in which the emission brightness of red, blue and green are different, the amount of current flowing through an EL element for displaying the color with the low emission  
10 brightness becomes larger than the amount of current flowing through an EL element for displaying the color with the relatively high emission brightness. By this, it is possible to display an image having an excellent balance among red, blue and green emission brightness.

Note that this embodiment can be used in combination with any other  
15 embodiments.

#### [Embodiment 10]

In this embodiment, an example of a structure of a light-emitting device of the present invention will be described with reference to Fig. 20.

An insulating film 906 is formed on a substrate 905, and there are formed  
20 thereon a p-channel TFT 901 and an n-channel TFT 902 included in a CMOS circuit of a driving circuit (source signal line driving circuit or gate signal line driving circuit), and a switching TFT 903 and a current controlling TFT 904 included in a pixel portion.

The p-channel TFT 901 included in the driving circuit includes a source

region 907, a drain region 909, and a channel forming region 908. Further, the p-channel TFT 901 includes the gate insulating film 906 on the channel forming region 908, and a gate electrode 922 on the gate insulating film 906. A first interlayer insulating film 927 is provided to cover the gate insulating film 906 and the gate electrode 922. Further, the p-channel TFT 901 includes a source wiring line 928 connected to the source region 907 and a drain wiring line 929 connected to the drain region 909, through contact holes provided in the gate insulating film 906 and the first interlayer insulating film 927.

The n-channel TFT 902 included in the driving circuit includes a source region 912, a drain region 910, and a channel forming region 911. Further, the n-channel TFT 902 includes the gate insulating film 906 on the channel forming region 911, and a gate electrode 923 on the gate insulating film 906. The first interlayer insulating film 927 is provided to cover the gate insulating film 906 and the gate electrode 923. Further, the n-channel TFT 902 includes a source wiring line 930 connected to the source region 912 and a drain wiring line 929 connected to the drain region 910, through contact holes provided in the gate insulating film 906 and the first interlayer insulating film 927.

The switching TFT 903 included in the pixel portion has a double gate structure. Note that in this embodiment, although the switching TFT 903 has the double gate structure, it may have a single gate structure or another multigate structure. The switching TFT 903 includes a source region 913, a drain region 917, channel forming regions 914 and 916, and an impurity addition region 915. Further, the switching TFT 903 includes the gate insulating film 906 on the channel forming regions 914 and 916, and gate electrodes 924 and 925 on the gate insulating film 906. The first interlayer insulating film 927 is provided to cover the gate insulating

film 906 and the gate electrodes 924 and 925. Further, the switching TFT 903 includes a source wiring line (source signal line) 931 connected to the source region 913 and a drain wiring line 932 connected to the drain region 917, through contact holes provided in the gate insulating film 906 and the first interlayer insulating film  
5 927.

Reference numeral 957 designates a gate wiring line (gate signal line), which electrically connects the gate electrode 924 of the switching TFT 903 to the gate electrode 925. The gate wiring line 957 may be formed of the same material as the gate electrodes 924 and 925 of the switching TFT 903 or may be formed of a  
10 different material. By forming the gate electrodes 924 and 925 from a material easy to precisely work, and forming the gate wiring line 957 from a material having resistance lower than the material forming the gate electrodes 924 and 925, it becomes possible to form a light-emitting device having higher definition and a large screen.

15 The current controlling TFT 904 included in the pixel portion has a single gate structure. Note that in this embodiment, although the current controlling TFT 904 has the single gate structure, it may have a double gate structure or another multigate structure. The current controlling TFT 904 includes a source region 918, a drain region 920, and a channel forming region 919. Further, the current  
20 controlling TFT 904 includes the gate insulating film 906 on the channel forming regions 919, and a gate electrode 926 on the gate insulating film 906. The first interlayer insulating film 927 is provided to cover the gate insulating film 906 and the gate electrode 926. Further, the current controlling TFT 904 includes a source wiring line 933 connected to the source region 918 and a drain wiring line 934  
25 connected to the drain region 920, through contact holes provided in the gate



insulating film 906 and the first interlayer insulating film 927.

A second interlayer insulating film 935 is formed to cover the first interlayer insulating film 927, the source wiring lines 928, 930, 931, and 933, and the drain wiring lines 929, 932, and 934. A third interlayer insulating film (flattening film)  
5 936 made of an organic resin is formed on the second interlayer insulating film 935.

A pixel electrode 937 connected to the drain wiring line 934 of the current controlling TFT 904 through a contact hole formed in the second interlayer insulating film 935 and the third interlayer insulating film 936 is formed on the third  
10 interlayer insulating film 936. In this embodiment, it is desirable that the pixel electrode 937 is formed of a transparent electrode, for example, ITO.

Besides, a bank 938 for separating EL layers or light-emitting layers between pixels is provided on the source wiring line 931. In this embodiment, although the bank 938 is provided on the source wiring line 931, the present invention is not  
15 limited to this. The bank 938 may be provided on the gate wiring line 957.

An EL layer 939 is provided on the pixel electrode 937. The EL layer can be formed using a well-known material. A cathode 940 is provided on the EL layer 939. The cathode 940 can be formed of a well-known material, and it was formed using MgAg in this embodiment.

20 It is desirable that the EL layer 939 and the cathodes 940 are continuously formed in the same chamber without opening to the air.

Since the light-emitting device having the structure of this embodiment does not include an LDD region, the operation speed is relatively high.

In the case where a voltage applied to the EL element becomes 10 V or less,  
25 preferably 5 V or less, since deterioration of the TFT due to the hot carrier effect

does not become a serious problem; the structure including no LDD regions set forth in this embodiment is effective in suppressing the number of fabricating steps.

[Embodiment 11]

5        In this embodiment, a description will be given of an example in the case where the present invention is applied to an actual light-emitting device using the above expressions 8 and 11 and which is different from the former embodiment.

      In this embodiment, a light-emitting device having a resolution of QVGA of  $320 \times 240$  and a size of 4 inches will be exemplified.

10       A pixel size of the 4-inch QVGA light-emitting device is about  $84 \mu\text{m} \times 252 \mu\text{m}$ . When an attempt to obtain constant brightness is made, the amount of current per unit area flowing through an EL element is determined. In this embodiment, it is made  $3 \text{ mA/cm}^2$  per unit area.

      Thus, a drain current  $I_d$  of a current controlling TFT included in each of  
15    pixels is expressed by the following expression 29.

[Expression 29]

      The above expression 29 indicates a value of the drain current  $I_d$  of the current controlling TFT when the opening ratio of the light-emitting device is made 100 %. Actually, in almost all cases, the opening ratio of the light-emitting device  
20    is not 100 %. As the opening ratio of the light-emitting device becomes small, the value of the actually required drain current  $I_d$  becomes large. For example, if the opening ratio of the light-emitting device of this embodiment is 30 %, the value of

the actually required drain current  $I_d$  is obtained by the following equation 30.

[Expression 30]

Since the light-emitting device used in this embodiment uses a bottom gate type current controlling TFT, when a mobility of the current controlling TFT is  $\mu$   
5  $= 50$  ( $\text{m}^2/\text{V}\cdot\text{sec}$ ) and a capacitance value of the gate capacitance is  $C_o = 2.4 \times 10^{-8}$  ( $\text{F}/\text{cm}^2$ ), a constant  $A$  is obtained from expression 31.

[Expression 31]

In this embodiment, a difference between emission brightness of the respective pixels is restricted within a range of, for example,  $\pm 5\%$ . When a gate voltage  
10  $V_{gs(\text{max})}$  immediately before the TFT is broken is made 25 V, and a value of a threshold voltage  $V_{th}$  is made 0 V, the following expressions 32 and 33 are obtained from the expressions 8 and 11.

[Expression 32]

[Expression 33]

15 In the light-emitting device of the present invention, the values of  $\Delta V_{th}$  and  $W/L$  are determined within the range where the above expression 32 or 33 is satisfied, and the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm 5\%$ .

It is generally desirable that the fluctuation  $\Delta V_{th}$  of the threshold value of the current controlling TFT is 0.1 V or less.

It is assumed that the fluctuation  $\Delta V_{th}$  of the threshold voltage is  $\Delta V_{th} \leq 0.1$  V by a fabricating process of the TFT. When  $\Delta V_{th} = 0.1$  V is substituted in the  
5 expression 33, the following expression 34 is obtained.

[Expression 34]

If the ratio  $W/L$  of the channel length  $L$  to the channel width  $W$  is determined so that the expression 34 is satisfied, the fluctuation of the drain current  $I_d$  can be suppressed to the range of  $\pm 5\%$ .

10 According to the above structure, in the light-emitting device of the present invention, the number of thin film transistors provided in each of pixels is made two to prevent a drop in the opening ratio, and it becomes possible to suppress uneven brightness due to fluctuation in the threshold voltage of current controlling TFTs included in the respective pixels.

15 Note that in this embodiment, although the description has been given of the example in which the fluctuation of the drain current  $I_d$  is suppressed to the range of  $\pm 5\%$ , the present invention is not limited to this numerical value.

[Embodiment 12]

In the present invention, external luminous quantum efficiency can be  
20 remarkably improved by using an EL material which can use phosphorescence from a triplet exciton for light emission. By this, it becomes possible to realize low power consumption, long lifetime, and light weight of an EL element.

Here, there is a report in which the triplet exciton is used and the external luminous quantum efficiency is improved. (T. Tsutsui, C. Adachi, S. Saito, Photochemical Processes in Organized Molecular Systems, ed. K. Honda, (Elsevier Sci. Pub., Tokyo, 1991) p. 437.)

- 5        A molecular formula of an EL material (coumarin pigment) reported in the above paper is as follows:

[Chemical Formula 1]

(M. A. Baldo, D.F.O'Brien, Y. You, A. Shoustikov, S. Sibley, M.E. Thompson, S.R. Forrest, Nature 395 (1988) p. 151.)

- 10       A molecular formula of an EL material (Pt complex) reported in the above paper is as follows:

[Chemical Formula 2]

- (M.A. Baldo, S. Lamansky, P.E. Burrows, M.E. Thompson, S.R. Forrest, Appl. Phys. Lett., 75 (1999) p. 4.) (T. Tsutsui, M.-J. Yang, M.Yahiro, K. Nakamura, T. Watanabe, T. Tsuchi, Y. Fukuda, T. Wakimoto, S. Mayaguchi, Jpn. Appl. Phys., 38 (12B) (1999) L1502.)
- 15

A molecular formula of an EL material (Ir complex) reported in the above paper is as follows:

[Chemical Formula 3]

As described above, if phosphorescence emission from the triplet exciton can be used, in principle, it becomes possible to realize the external luminous quantum efficiency 3 to 4 times as high as the case of using fluorescence from a single exciton.

- 5        Note that the structure of this embodiment can be freely combined with any structure of the embodiments 1 to 11 and can be carried out.

[Embodiment 13]

A light-emitting device has superior visibility in bright locations in comparison to a liquid crystal display device because it is of a self-emitting type, and moreover  
10    viewing angle is wide. Accordingly, it can be used as a display portion for various electronic apparatuses. For example, it is appropriate to use the light-emitting device of the present invention as a display portion of an EL display (a display incorporating the light-emitting device in its casing) having a diagonal equal to 30 inches or greater (typically equal to 40 inches or greater) for appreciation of TV  
15    broadcasts by a large screen.

Note that all displays exhibiting (displaying) information such as a personal computer display, a TV broadcast reception display, or an advertisement display are included as the EL display. Further, the light-emitting device of the present invention can be used as a display portion of the other various electronic  
20    apparatuses.

The following can be given as examples of such electronic apparatuses: a video camera; a digital camera; a goggle type display (head mounted display); a car navigation system; an audio reproducing device (such as a car audio system, an audio compo system); a notebook personal computer; a game equipment; a portable

information terminal (such as a mobile computer, a mobile telephone, a mobile game equipment or an electronic book); and an image reproduction device provided with a recording medium (specifically, a device which performs reproduction of a recording medium and is provided with a display which can display those images, such as a digital video disk (DVD)). In particular, because portable information terminals are often viewed from a diagonal direction, the wideness of the field of vision is regarded as very important. Thus, it is preferable that the light-emitting device is employed. Examples of these electronic instruments are shown in Figs. 16A through 17B.

10        Fig. 16A illustrates an EL display which includes a frame 2001, a support table 2002, a display portion 2003, or the like. The light-emitting device in accordance with the present invention can be used as the display portion 2003. The light-emitting device is of a self-emitting type and therefore requires no back light. Thus, the display portion thereof can have a thickness thinner than that of the liquid  
15        crystal display device.

      Fig. 16B illustrates a video camera which includes a main body 2101, a display portion 2102, an audio input portion 2103, operation switches 2104, a battery 2105, an image receiving portion 2106, or the like. The light-emitting device in accordance with the present invention can be used as the display portion 2102.

20        Fig. 16C illustrates a portion (the right-half piece) of an electro-optical device of head-mounted type which includes a main body 2201, signal cables 2202, a head mount band 2203, a screen portion 2204, an optical system 2205, a display portion 2206, or the like. The light-emitting device in accordance with the present invention can be used as the display portion 2206.

25        Fig. 16D illustrates an image reproduction apparatus which includes a

recording medium (more specifically, a DVD reproduction apparatus), which includes a main body 2301, a recording medium (a DVD or the like) 2302, operation switches 2303, a display portion (a) 2304, another display portion (b) 2305, or the like. The display portion (a) 2304 is used mainly for displaying image information, while the display portion (b) 2305 is used mainly for displaying character information. The light-emitting device in accordance with the present invention can be used as these display portions (a) and (b), 2304 and 2305. The image reproduction apparatus including a recording medium further includes a domestic game equipment or the like.

10 Fig. 16E illustrates a goggle type display (head-mounted display) which includes a main body 2401, a display portion 2402, an arm portion 2403. The light-emitting device in accordance with the present invention can be used as the display portion 2402.

Fig. 16F illustrates a personal computer which includes a main body 2501, a frame 2502, a display portion 2503, a key board 2504, or the like. The light-emitting device in accordance with the present invention can be used as the display portion 2503.

Note that if emission brightness of an EL material becomes higher in the future, it will be applicable to a front-type or rear-type projector in which light including output image information is enlarged by means of lenses or the like to be projected.

The above mentioned electronic apparatuses are more likely to be used for display information distributed through a telecommunication path such as Internet, a CATV (cable television system), and in particular likely to display moving picture information. The light-emitting device is suitable for displaying moving pictures



since the EL material can exhibit high response speed.

Further, since a light emitting portion of the light-emitting device consumes power, it is desirable to display information in such a manner that the light emitting portion therein becomes as small as possible. Accordingly, when the light-emitting  
5 device is applied to a display portion which mainly displays character information, e.g., a display portion of a portable information terminal, and more particular, a portable telephone or an audio reproducing device, it is desirable to drive the light emitting device so that the character information is formed by a light-emitting portion while a non-emission portion corresponds to the background.

10 Fig. 17A illustrates a portable telephone which includes a main body 2601, an audio output portion 2602, an audio input portion 2603, a display portion 2604, operation switches 2605, and an antenna 2606. The light-emitting device in accordance with the present invention can be used as the display portion 2604. Note that the display portion 2604 can reduce power consumption of the portable  
15 telephone by displaying white-colored characters on a black-colored background.

Further, Fig. 17B illustrates a sound reproduction device, specifically, a car audio equipment in concrete term, which includes a main body 2701, a display portion 2702, and operation switches 2703 and 2704. The light-emitting device in accordance with the present invention can be used as the display portion 2702.  
20 Although the car audio equipment of the mount type is shown in the present embodiment, the present invention is also applicable to a portable type or domestic sound reproducing device. The display portion 2702 can reduce power consumption by displaying white-colored characters on a black-colored background, which is particularly advantageous for the portable type sound reproduction device.

25 As set forth above, the present invention can be applied variously to a wide

range of electronic instruments in all fields. The electronic apparatuses in the present embodiment can be obtained by utilizing a light-emitting device having the configuration in which the structures in Embodiments 1 through 12 are freely combined.

5        According to the present invention, in the case where the fluctuation  $\Delta V_{th}$  of the threshold voltage is fixed by a fabricating process of a TFT, from the value of the fluctuation  $\Delta V_{th}$  of the threshold voltage, the range of the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$  is determined by the expression 14.

      Besides, according to the present invention, in the case where the value of the  
10      ratio  $W/L$  of the channel width  $W$  to the channel length  $L$  is fixed by a problem of design, from the value of the ratio  $W/L$  of the channel width  $W$  to the channel length  $L$ , the range of the fluctuation  $\Delta V_{th}$  of the threshold voltage is determined by the expression 15.

      According to the above structure, in the light-emitting device of the present  
15      invention, the number of thin film transistors provided in each of the pixels is made two to prevent a drop in the opening ratio, and it becomes possible to suppress uneven luminance due to fluctuation in the threshold voltage of current controlling TFTs included in the respective pixels.